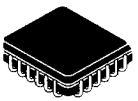
# DVSR Codec

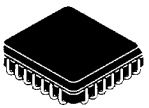
## DESCRIPTION

The MX802 Data/Voice Storage and Retrieval (DVSR) Codec contains a Continuosly Variable Slope Delta Modulation (CVSD) encoder and decoder, as well as control and timing circuitry for up to 4 Mbits of external DRAM. As a member of the DBS 800 series, it also contains interface and control logic for the "C-BUS" serial interface.

MX802J
28-pin CDIP



MX802LH
PLCC-24



MX802LH8
PLCC-28

When used with external DRAM, the MX802 has four primary functions:

- **Speech Storage**
  Speech signals present at the Audio Input may be digitized by the CVSD encoder. The resulting bit stream is stored in DRAM. This process also provides readings of the speech signal power level. These readings are used by the system microcontroller for pause reduction.
- **Speech Playback**
  Digitzed speech may be read from DRAM and converted back into analog form by the CVSD decoder.
- **Data Storage**
  Digital data derived via the C-BUS from the Modem or system data may be stored in DRAM.
- **Data Recovery**
  Digital data may be read from DRAM and sent over the C-BUS to the system microcontroller and Modem.

Speech storage and playback may be performed concurrently with data storage or retrieval.

The MX802 may also be used without DRAM (as a "stand alone" CVSD codec), in which case direct access is provided to the CVSD Codec digital data and clock signals. All functions are controlled by C-BUS commands from the system microcontroller.

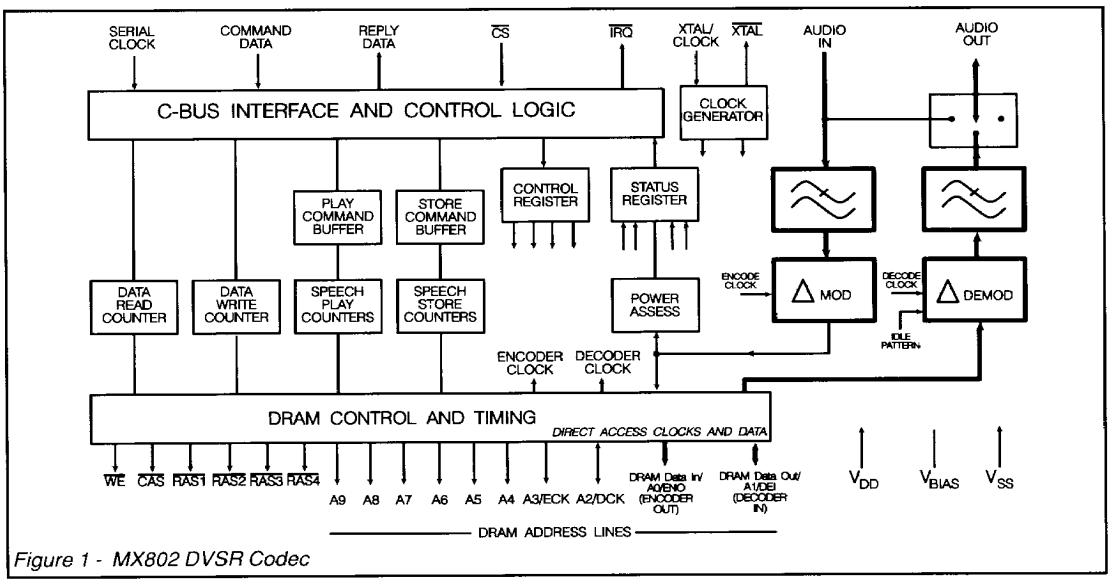



*Figure 1 - MX802 DVSR Codec*

The storage, recovery and replay functions of the MX802 can be used for:

- Answering Machine applications, where an incoming speech message is stored for later recall.
- Busy Buffering, in which an outgoing speech message is stored temporarily until the transmit channel becomes free.
- Automatic transmission of pre-recorded alarm or status announcements.
- Time Domain Scrambling of speech messages.
- VOX control of transmitter functions.
- Temporary Data Storage applications, such as buffering of over-air data transmissions.

On-chip the Delta Codec is supported by input and output analog switched-capacitor filters and audio output switching circuitry. The DRAM control and timing circuitry provides all the necessary address, control and refresh signals to interface to external DRAM. The MX802 DVSR Codec is a low-power 5-volt CMOS LSI device. It is offered in 24- and 28-lead SMT packages, as well as a 28-pin DIP package.

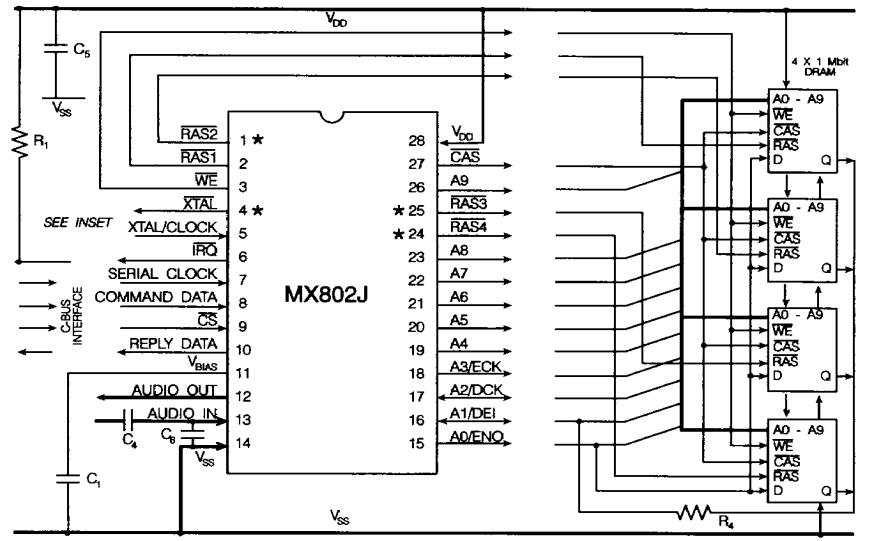
## Pin Function Table

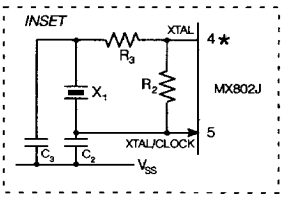
| Pin | | Function |
|---|---|---|
| J/LH8 | LH | |
| 1 | | **Row Address Strobe 2 ($\overline{RAS2}$):** This pin should be connected to the Row Address Strobe input of the second 1 Mbit DRAM chip (if used). |
| 2 | 1 | **Row Address Strobe 1 ($\overline{RAS1}$):** This pin should be connected to the Row Address Strobe input of the first DRAM chip. |
| 3 | 2 | **Write Enable ($\overline{WE}$):** The DRAM Read/Write control pin. A logic "1" (high) sets the read mode; a logic "0" (low) sets the write mode. This function is driven by C-BUS commands. |
| 4 | | **$\overline{Xtal}$:** This is the output of the 4.0 MHz on-chip clock oscillator. External components are required at this output when a Xtal is used. A Xtal cannot be used with the 24-pin version. |
| 5 | 3 | **Xtal/Clock:** This is the input to the on-chip clock oscillator inverter. A 4.0MHz Xtal or externally derived clock should be connected here (see component diagram). This clock provides timing for on-chip elements, filters, etc. A Xtal cannot be used with the 24-pin version. Various Xtal frequencies can be used with this device; see Table 3 for sampling rate variations. |
| 6 | 4 | **Interrupt Request ($\overline{IRQ}$):** The output of this pin indicates an interrupt condition to the microcontroller by going to logic "0." This is a "wire-or able" output, enabling the connection of up to 8 peripherals to 1 interrupt port on the microcontroller. This pin is an open drain output. It therefore has a low impedance pulldown to logic "0" when active and a high impedance when inactive. Conditions indicated by this function are Power Reading Ready, Play Command Complete and Store Command Complete. |
| 7 | 5 | **Serial Clock:** This is the C-BUS serial clock input. This clock, produced by the microcontroller, is used for transfer timing of command data to and from the DVSR Codec. See timing diagrams (page 11). Clock rate requirements vary for different MX802 functions. |
| 8 | 6 | **Command Data:** This is the C-BUS serial data input from the microcontroller. Data is loaded to this device in 8-bit bytes, MSB (bit 7) first, and LSB (bit 0) last, synchronized to the Serial Clock. See timing diagrams. |
| 9 | 7 | **Chip Select ($\overline{CS}$):** The C-BUS data transfer control function, this input is provided by the microcontroller. Command Data transfer sequences are initiated, completed or aborted by the $\overline{CS}$ signal. See timing diagrams. |
| 10 | 8 | **Reply Data:** This is the C-BUS serial data output to the microcontroller. The transmission of Reply Data bytes is synchronized to the Serial Data Clock under the control of the Chip Select input. This 3-state output is held at high impedance when not sending data to the microcontroller. See timing diagrams. |

## Pin Function Table

| Pin | | Function |
|---|---|---|
| J/LH8 | LH | |
| 11 | 9 | $V_{BIAS}$: This is the output of the on-chip analog circuitry bias system, held internally at $V_{DD}/2$. This pin should be decoupled to $V_{SS}$ by capacitor $C_1$. See Figure 2. |
| 12 | 10 | **Audio Out:** This is the analog signal output. |
| 13 | 11 | **Audio In:** This is the audio (speech) input. The signal to this pin must be a.c. coupled by capacitor $C_4$. For optimum noise performance this input should be driven from a source impedance of less than 100Ω. |
| 14 | 12 | $V_{SS}$: Negative Supply (GND). |
| 15 | 13 | **DRAM Data In/A0/Direct Access -- Encoder Out (ENO):** This is the DRAM data input pin and address line, A0. With no DRAM used, this output is available in a Direct Access mode as the Delta Encoder digital data Output. Direct Access control is achieved by Control Register byte 1, bit 7. |
| 16 | 14 | **DRAM Data Out/A1/Direct Access -- Decoder In (DEI):** This is the DRAM data output pin and address line, A1. With no DRAM used, this pin is available in a Direct Access mode as the Delta Decoder digital data Input. Direct Access control is achieved by Control Register byte 1, bit 6. |
| 17 | 15 | **DRAM A2/Direct Access -- Decoder Clock (DCK):** This is the DRAM address line A2. With no DRAM employed, this pin is available in a Direct Access mode as the Delta Decoder Clock Input. Direct Access control is achieved by Control Register byte 1, bit 6. |
| 18 | 16 | **DRAM A3/Direct Access -- Encoder Clock (ECK):** This is the DRAM address line A3. With no DRAM employed, this pin is available in a Direct Access mode as the Delta Encoder Clock Output. Direct Access control is achieved by Control Register byte1, bit 6. |
| 19 | 17 | **DRAM A4:** DRAM address line A4. |
| 20 | 18 | **DRAM A5:** DRAM address line A5. |
| 21 | 19 | **DRAM A6:** DRAM address line A6. |
| 22 | 20 | **DRAM A7:** DRAM address line A7. |
| 23 | 21 | **DRAM A8:** DRAM address line A8. |
| 24 | 22 | **Row Address Strobe 4 ($\overline{RAS4}$):** This pin should be connected to the Row Address Strobe input of the fourth 1 Mbit DRAM chip (if used). |
| 25 | | **Row Address Strobe 3 ($\overline{RAS3}$):** This pin should be connected to the Row Address Strobe input of the third 1 Mbit DRAM chip (if used). |
| 26 | | **DRAM A9:** This is DRAM address line A9. This pin is not connected when a 256 kbit DRAM is used. Note: To simplify PCB layout, the DRAM address inputs A0-A9 may be connected in any physical order to the DVSR Codec output pins A0-A9. |
| 27 | 23 | **Column Address Strobe ($\overline{CAS}$):** This is the DRAM Column Address Strobe pin. It should be connected to the $\overline{CAS}$ pins of all DRAM chips. |
| 28 | 24 | $V_{DD}$: Positive supply. A single, stable +5 volt supply is required. The stability of all levels in this DVSR Codec are dependent upon this supply. |

# External Components




| Component | Value | | |
|---|---|---|---|
| $R_1$ | 22.0kΩ | $C_4$ | 1.0µF |
| $R_2$ | 1.0MΩ | $C_5$ | 1.0µF |
| $R_3$ | See Note 1 | $C_6$ | .001µF |
| $R_4$ | 1.0kΩ | $X_1$ | 4.00MHz |
| $C_1$ | 1.0µF | or | 4.032MHz |
| $C_2$ | 33.0pF | or | 4.096MHz |
| $C_3$ | 33.0pF | Tolerance: R = ±10%, C = ±20% | |

*Figure 2 - Recommended External Component and DRAM Connections*

*See Note 3

**Notes**

1. Xtal circuitry shown in Inset is in accordance with MX-COM's Application Note on Standard and DBS 800 Crystal Oscillators (p. 354).

2. External Xtal circuitry is not applicable to the 24 pin/lead versions of this device. Only an externally derived clock input can be used.

3. Functions whose pins are marked with an asterisk* in Figure 2 are not available on the 24-pin/lead versions of this device. Pin numbers illustrated are for 28-pin versions.

4. Table 3 details the actual encoder/decoder sample rates available using the Xtal frequencies recommended above.

5. Resistor $R_1$ is used as the DBS 800 system common pullup for the C-BUS Interrupt Request ($\overline{IRQ}$) line. The optimum value will depend on the circuitry connected to the $\overline{IRQ}$ line. Up to 8 peripherals may be connected to this line.

6. Recommended DRAM Parameters:
256 kbit x 1 or 1 Mbit x 1 Dynamic Random Access Memory with "CAS before RAS" refresh mode. Maximum Row address access time = .200 µsec.

Example DRAM types:

| | |
|---|---|
| 256kbit (262,144 bits) | |
| Texas Instruments | TMS4256-20 |
| Hitachi | HM51256-15 |
| 1Mbit (1,048,576 bits) | |
| Texas Instruments | TMS4C1024-15 |
| Hitachi | HM511000-15 |

7. Figure 2 above shows connections to 4 x 1 Mbit sections of DRAM. If desired, to simplify PCB layout, the DRAM inputs A0-A8 may be connected in any order to the MX802 DVSR Codec output pins A0-A8. Connections to 256 kbit DRAM are similar, but A9 is left unconnected.

8. When using the MX802 "stand alone" (Direct Access), no DRAM sections should be connected.

# Controlling Protocol

Control of the functions of the MX802 DVSR Codec is by a group of Address/Commands (A/Cs) and appended instructions or data to and from the system microcontroller (See Figure 4). The use and content of these instructions is detailed in the following pages.

| Command Assignment | Address/Command (A/C) Byte Hex. | Binary MSB LSB | Data Byte(s) |
|---|---|---|---|
| General Reset | 01 | 0 0 0 0 0 0 0 1 | |
| Write to Control Register | 60 | 0 1 1 0 0 0 0 0 | + 2 byte instruction to Control Register |
| Read Status Register | 61 | 0 1 1 0 0 0 0 1 | + 1 byte reply from Status Register |
| Store "N" pages. Start page "X" | 62 | 0 1 1 0 0 0 1 0 | + 2 bytes Command -- Immediate |
| Store "N" pages. Start page "X" | 63 | 0 1 1 0 0 0 1 1 | + 2 bytes Command -- Buffered |
| Play "N" pages. Start page "X" | 64 | 0 1 1 0 0 1 0 0 | + 2 bytes Command -- Immediate |
| Play "N" pages. Start page "X" | 65 | 0 1 1 0 0 1 0 1 | + 2 bytes Command -- Buffered |
| Write Data. Start page "P" | 66 | 0 1 1 0 0 1 1 0 | + 2 bytes "P" + Write Data |
| Read Data. Start page "P" | 67 | 0 1 1 0 0 1 1 1 | + 2 bytes "P" + Read Data |
| Write Data -- Continue | 68 | 0 1 1 0 1 0 0 0 | + Write data |
| Read Data -- Continue | 69 | 0 1 1 0 1 0 0 1 | + Read data |

*Table 1 - C-BUS Address/Commands*

## Address/Commands

Instruction and data transactions to and from this device consist of an Address/Command (A/C) byte followed by further instruction/data or a status/data reply.

Control and configuration is by writing instructions from the microcontroller to the Control Register ($60_H$). Reporting of MX802 configurations is by reading the Status Register ($61_H$).

## Operation with DRAM

The MX802 can operate with up to 4 Mbits of Dynamic RAM (DRAM). When used with DRAM, the MX802 performs four main functions under the control of commands received over the C-BUS interface from the microcontroller:

**Stores Speech:** The MX802 stores speech by digitally encoding the analog input signal and writing the resulting digital data into the associated DRAM.

**Plays Speech:** The MX802 plays back stored speech by reading the digital data stored in the DRAM and decoding it to provide an analog output signal.

**Writes Data:** The MX802 writes data sent over the C-BUS from the microcontroller to DRAM.

**Reads Data:** The MX802 reads data from DRAM, sending it to the microcontroller over the C-BUS.

Data is directed to and from DRAM by the on-chip DRAM Controller.

## Speech

The CVSD encoder and decoder sampling rates are independently set via the Control Register (see Table 2) to 16, 25, 32, 50 or 64 kbits/s. This allows the user to choose between speech quality and storage time while providing for time compression or expansion of the speech signals.

The DVSR Codec can handle from 256 kbits to 4 Mbits of DRAM, giving, in the case of the 32 kbit/s sampling rate, from 8 to 131 seconds of speech storage.

For speech storage purposes, the memory is divided into "pages" of 1024 bits each, corresponding to 32ms at a 32 kbit/s sampling rate.

| | |
|---|---|
| A 256 kbit DRAM contains | 256 "pages." |
| A 1 Mbit DRAM contains | 1024 "pages." |
| A 4 Mbit DRAM contains | 4096 "pages." |

When used without DRAM, the decoder sampling rate (8-64 kbits/s) is determined by an external clock source applied to the Decoder Clock pin.

### Store and Play Speech Commands

Speech storage and playback may take place simultaneously. These commands are transmitted, via C-BUS, to the MX802 in the following form:

STORE OR PLAY "N" (1024-bit) PAGES ( of encoded speech data) STARTING AT PAGE "X."

"N" can be any number between 1 and 16. "X" can be any number from 0 to 4095 (4Mbit DRAM), as shown below. Preceded by A/C, this command writes 16 bits (byte 1 and byte 0) of data from the microcontroller to the Store or Play Command Buffer.

| MSB BYTE 1 | | | | | | | | BYTE 0 LSB | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| N | | | | | | | | X | | | | | | | |

### Speech Store Commands

$62_H$ STORE "N" PAGES – START PAGE "X" (immediate)
$63_H$ STORE "N" PAGES – START PAGE "X" (buffered)

The digitized speech from the CVSD encoder is stored in consecutive DRAM locations with the Speech Store Counters sequencing through the DRAM addresses and counting the number of complete pages stored since the start of the execution of the command.

As soon as the command has terminated, the following events take place:

1. The Store Command Complete bit in the Status Register (Table 5) is set.

2. An Interrupt Request ($\overline{IRQ}$) is sent, if enabled, to the microcontroller.

3. The next speech storage command (if present) is immediately taken from the Store Command Buffer and execution of the new command commences.

**Speech Playback** is controlled by similar commands using the Speech Play Counters and Play Command Buffer:

$64_H$ PLAY "N" PAGES -- START PAGE "X" (immediate)
$65_H$ PLAY "N" PAGES -- START PAGE "X" (buffered).

As soon as the Play Command has completed, the "Play Command Complete" bit in the Status Register is set, and an Interrupt Request is generated (if enabled).

If no "next" command is waiting in the Play Command Buffer when a speech play command finishes, a continuous idle code (0101....0101) will be fed to the delta decoder.

Speech data is stored or recovered at the selected Encode or Decode sample rate (Table 3). Store or Play Command Complete bits in the Status Register are cleared by the next Store or Play Command received from the microcontroller, or by a General Reset ($01_H$).

Interrupts are cleared by reading the Status Register:

$61_H$ READ STATUS REGISTER (Table 5).

To provide continuity of speech commands, both Store and Play Commands can be presented to eh MX802 in one of two formats: *immediate or buffered.*

An *immediate* command will be started on completion of its loading, irrespective of the condition of the current command.

A *buffered* command will begin after the completion of the current Store or Play command, unless Speech Synchronization Bits (Control Register) are set.

## Speech...

Buffering of commands lets the DVSR Codec execute a series of commands without intervening gaps even though the microcontroller may take several milliseconds to respond to each "Command Complete" Interrupt Request.

In either case, the Store or Play Command Complete bit of the status register will be cleared.

**Store/Play Speech Synchronization (Table 4)**

This capability is provided primarily for Time Domain Scrambling applications.

Speech Synchronization bits in the Control Register will produce the effects described below:

**No Speech Sync Set:** Store and Play operations may take place completely independently.

**Store after Play:** The next buffered store command will start on completion of a play command, while the next play command sequence (if any) continues normally.

**Play after Store:** The next buffered play command will start on completion of a store command, while the next store command sequence (if any) continues normally.

These actions will continue while Speech Sync bits are set.

## Data Handling

For the purpose of storing data sent via C-BUS from the microcontroller, the memory (DRAM) is divided into "data pages" of 64 bits (8 bytes).

| | |
|---|---|
| A 256kbit DRAM contains | 4096 data pages. |
| A 1Mbit DRAM contains | 16384 data pages. |
| 4Mbit DRAM contains | 65536 data pages. |

In accordance with C-BUS timing specifications, data is handled 8 bits (1 byte) at a time, although any number of 8-bit blocks of data may be written to or read from the DRAM by a single command.

Data transfer is terminated by the Chip Select line going to a logic "1."

**Write Data**

$66_H$ WRITE DATA -- START PAGE "P"

This command sets the Data Write Counter to "P" page, and then writes data bytes to successive DRAM locations, incrementing the Data Write Counter by 1 for each bit received via the C-BUS.

The Start Page, "P," is indicated by loading a 2-byte word after the relevant Address/Command byte. This 16-bit word allows data page addresses from 0 to 65535 (4Mbits DRAM).

$68_H$ WRITE DATA CONTINUE

This command writes data bytes to successive DRAM locations determined by the Data Write Counter, incrementing the counter by 1 for each bit received over the C-BUS.

**Read Data**

$67_H$ READ DATA -- START PAGE "P"

This command sets the Data Read Counter to "P," page, and then reads data bytes from successive DRAM locations, sending them to the microcontroller as Reply Data bytes. The Data Read Counter is incremented by 1 for each bit read.

$69_H$ READ DATA CONTINUE

This command reads data bytes from successive DRAM locations determined by the Data Read Counter, incrementing the counter by 1 for each bit read.

**C-BUS Data Transfer Limitations**

For those commands which transfer data over the C-BUS between DRAM and the microcontroller (Write and Read data), the C-BUS serial clock rate is limited to a maximum of:

125kHz if the VSR Codec is executing store and play commands.

250kHz if no speech Store or Play commands are active.

This limitation is due to the rate at which data goes into and out of the DRAM. All other commands and replies (Control, Status, Reset) may use a maximum clock rate of 500kHz. See Figure 4.

## DRAM Speech Capacity

28-pin/lead versions of the MX802 may be used with a single 256kbit DRAM, or with up to 4 x 1Mbit of DRAM. 24-pin/lead versions may only be used with a single 256kbit or 1Mbit DRAM. The different encode and decode sampling clock rates available enable the user to set voice store and play times against recovered speech quality. Table 2 gives information on storage capacity and Store/Playback times. Speech data can be replayed at a different sample rate or in a reversed sequence (see Control Register for details).

| DRAM Size | Available Bits | Speech Pages | Nominal Sample Rates (kbit/s) 16 | 25 | 32 | 50 | 64 |
|---|---|---|---|---|---|---|---|
| 256kbits | 262144 | 256 | 16.0 | 10.0 | 8.0 | 5.0 | 4.0 |
| 1024k | 1048576 | 1024 | 65.0 | 42.0 | 32.0 | 20.0 | 16.0 |
| 2Mbits | 2097152 | 2048 | 131.0 | 84.0 | 65.0 | 42.0 | 32.0 |
| 3M | 3145728 | 3072 | 196.0 | 126.0 | 98.0 | 63.0 | 49.0 |
| 4M | 4194304 | 4096 | 262.0 | 168.0 | 131.0 | 84.0 | 65.5 |
| | | | Store and Play Times (seconds) | | | | |

*Table 2 - Sampling Clock Rates vs Speech Storage/Playback Times*

## Encoder and Decoder Sampling Clocks

Encoder and decoder sampling clock rates are programmable via the Control Register. Table 3 shows the range of sampling rates available for different Xtal/clock input frequencies and the counter ratios used to produce them. Consideration should be given to the effect of different Xtal/clock frequencies upon the audio frequency performance of the device.

| Control Register *Byte 0, Bits* 5 4 3 Dec. / 2 1 0 Enc. | Internal Counter Division Ratio | Xtal.clock Frequency (MHz) 4.0 | 4.032 | 4.096 |
|---|---|---|---|---|
| | | Sampling Rate kbits/s | | |
| 0 1 1 | 256 | 15.625 | 15.75 | 16.0 |
| 1 0 0 | 160 | 25.0 | 25.20 | 25.60 |
| 1 0 1 | 128 | 31.25 | 31.50 | 32.0 |
| 1 1 0 | 80 | 50.0 | 50.4 | 51.20 |
| 1 1 1 | 64 | 62.50 | 63.0 | 64.0 |

*Table 3 - Sampling Clock Rates Available*

With respect to using a single Xtal/clock frequency for all DBS 800 devices in use, it should be noted that

(a) a 4.032MHz Xtal/clock input will produce an accurate 1200-baud rate for the MX809 MSK Modem.

(b) a 4.096MHz Xtal/clock input will generate exactly 16kb/s, 32kb/s and 64kb/s Codec sampling clock rates.

## "Write to Control Register" - Address/Command $60_H$, followed by 2 bytes of Command Data

| Setting | Function |
|---|---|
| ***Byte 1*** | ***First Byte for Transmission*** |
| ***(MSB) Bit 7*** | Not used - Set to "0" |
| ***6*** | **Direct Access** |
| *1* | -- Encoder Data out to A0/ENO<br>-- Encoder Clock to A3/ECK<br>-- Decoder Input from A1/DEI<br>-- Decoder Clock from A2/DCK |
| 0 | Normal Operation |
| ***5*** | **Play Counter** |
| 1 | Decrement |
| 0 | Increment |
| ***4*** | **DRAM Control** |
| 1 | Disable DRAM |
| 0 | Enable DRAM |
| ***3*** | **Codec Powersave** |
| 1 | Powersave MX802 |
| 0 | MX802 Enable |
| ***2*** | **Store Command Interrupt** |
| 1 | Enable Interrupt |
| 0 | Disable |
| ***1*** | **Play Command Interrupt** |
| 1 | Enable Interrupt |
| 0 | Disable |
| ***0*** | **Power Reading Interrupt** |
| 1 | Enable Interrupt |
| 0 | Disable |
| ***Byte 0*** | ***Last Byte for Transmission*** |
| **(MSB)** | |
| ***7 6*** | **Store/Play Speech Sync.** |
| 0 0 | No Sync |
| 0 1 | No Sync |
| 1 0 | Sync - Play after Store |
| 1 1 | Sync - Store after Play |
| ***5 4 3*** | **Decoder Control** |
| 0 0 0 | Off - Audio output from LPF |
| 0 0 1 | Off - Audio bypass |
| 0 1 0 | Off - Audio output at high Z |
| 0 1 1 | On - Sampling Rate 16kbit/s |
| 1 0 0 | On - 25kbit/s |
| 1 0 1 | On - 32kbit/s |
| 1 1 0 | On - 50kbit/s |
| 1 1 1 | On - 64kbit/s |
| ***2 1 0*** | **Encoder Control** |
| 0 0 0 | Off |
| 0 0 1 | Off |
| 0 1 0 | Off |
| 0 1 1 | On - Sampling Rate 16kbit/s |
| 1 0 0 | On - 25kbit/s |
| 1 0 1 | On - 32kbit/s |
| 1 1 0 | On - 50kbit/s |
| 1 1 1 | On - 64kbit/s |

*Table 4 - Control Register*

**General Reset**

Upon power-up the bits in the MX802 registers will be random (either 0 or 1). A General Reset Command ($01_{HEX}$) will be required to reset all devices on the C-BUS. It has the following effect on the MX802:

| | |
|---|---|
| Control Register | Set to $00_H$ |
| Status Register | Set to $00_H$ |
| Clear Store and Play Command Buffers | |

**Direct Access**

External circuitry is allowed direct access to the Delta Codec data and sampling clocks, disabling the DRAM timing circuitry. This permits the Delta Codec section of the MX802 to be used as a Delta Modulation voice encoder and decoder.

Input audio is encoded and made available at the Encoder Out (ENO) pin. Speech data input to the Decoder In (DEI) pin is decoded to give voice-band audio at the Audio Output.

The decoder sampling clock rate (8kbit/s to 64kbit/s) must be provided from an external source to the Decoder Clock (DCK) pin.

The encoder internal sampling clock rate is available to external circuitry at the Encoder Clock Out (ECK) pin.

**Play Counter**

The Play Counter direction may be reversed to decrement memory locations. This can be used in a scrambling system by replaying speech data in reverse order.

**DRAM Control**

A logic "1" will disable the DRAM Control Timing circuits and associated counters. The C-BUS Interface, Clock Generator, Delta Codec and filters remain active. This bit should be set to logic "1" when the MX802 is used in the Direct Access Mode.

Minimum DVSR Codec power consumption is achieved by setting both DRAM Control and Powersave bits to logic "1."

**Codec Powersave**

A logic "1" puts the Delta Codec and filters into Powersave Mode. The Audio Output pin is at high impedance and $V_{BIAS}$ is maintained. The Clock Generator, C-BUS Interface, DRAM Control and Timing remain active.

**Command Interrupt Enable**

A logic "1" set at the relevant bit will enable Interrupt Requests to the microcontroller when that command operation is complete.

**Store and Play Speech Synchronization**

This is intended primarily for Time Domain Scrambling (See "Speech" under Controlling Protocol).

**Decoder and Encoder Control**

This individually sets decoder and encoder sampling clock rates, as well as the source of the audio output.

## "Read Status Register" - Address/Command $61_H$, followed by 1 byte of Reply Data

| Reading | | | | | Function |
|---|---|---|---|---|---|
| MSB Bit 7 | | | | | |
| 1 | | | | | **Power Reading** Ready |
| **6** | | | | | |
| 1 | | | | | **Store Command** Complete |
| **5** | | | | | |
| 1 | | | | | **Play Command** Complete |
| **4** | **3** | **2** | **1** | **0** | **Power Register Compand Pulses** |
| 0 | 0 | 0 | 0 | 0 | No Compand |
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 0 | 1 | 1 | 3 |
| 0 | 0 | 1 | 0 | 0 | 4 |
| 0 | 0 | 1 | 0 | 0 | 5 |
| 0 | 0 | 1 | 1 | 0 | 6 |
| 0 | 0 | 1 | 1 | 1 | 7 |
| 0 | 1 | 0 | 0 | 0 | 8 |
| 0 | 1 | 0 | 0 | 1 | 10 |
| 0 | 1 | 0 | 1 | 0 | 12 |
| 0 | 1 | 0 | 1 | 1 | 14 |
| 0 | 1 | 1 | 0 | 0 | 16 |
| 0 | 1 | 1 | 0 | 1 | 18 |
| 0 | 1 | 1 | 1 | 0 | 20 |
| 0 | 1 | 1 | 1 | 1 | 22 |
| 1 | 0 | 0 | 0 | 0 | 24 |
| 1 | 0 | 0 | 0 | 1 | 32 |
| 1 | 0 | 0 | 1 | 0 | 40 |
| 1 | 0 | 0 | 1 | 1 | 48 |
| 1 | 0 | 1 | 0 | 0 | 56 |
| 1 | 0 | 1 | 0 | 1 | 64 |
| 1 | 0 | 1 | 1 | 0 | 72 |
| 1 | 0 | 1 | 1 | 1 | 80 |
| 1 | 1 | 0 | 0 | 0 | 88 |
| 1 | 1 | 0 | 0 | 1 | 128 |
| 1 | 1 | 0 | 1 | 0 | 192 |
| 1 | 1 | 0 | 1 | 1 | 256 |
| 1 | 1 | 1 | 0 | 0 | 320 |
| 1 | 1 | 1 | 0 | 1 | 384 |
| 1 | 1 | 1 | 1 | 0 | 448 |
| 1 | 1 | 1 | 1 | 1 | 512 |

*Table 5 - Status Register*

### Interrupts

If enabled by the Control Register, an Interrupt Request ($\overline{IRQ}$), is produced by the MX802 to report the following actions:

Power Reading Ready
Store Command Complete
Play Command Complete

When an Interrupt is produced, the Status Register must be read to determine the source of the interrupt. This action will clear the interrupt condition.

The **Store Command Complete** bit (and an interrupt) is set on completion of a Store Command. This bit is cleared by loading the next Store Command, or by a General Reset Command ($01_H$).

The **Play Command Complete** bit (and an interrupt) is set on completion of a Play Command. This bit is cleared by loading the next Play Command, or by a General Reset Command ($01_H$).

The **Power Reading Ready** bit (and an interrupt) is set for every 1024 voice-data bits (1 page) from the Encoder. This bit is cleared after reading the Status Register, or by a General Reset Command ($01_H$).

### Power Register

The power assessment element shown in Figure 1 assesses the input signal power for each encoded "page" (i.e. every 1024 encoder output bits) by counting the number of "compand bits" (000 or 111 sequences in the output bit stream) produced during that page.

At the end of each "page" the power reading ready bit of the status register is set, and an interrupt request is generated (if enabled). The resulting count is converted into a 5-bit quasi-logarithmic form. The Power Register reading is interpreted as follows:

00000 represents 0 compand bits
00001 represents 1 compand bit
11111 represents 512 compand bits, the maximum.

This power reading is placed in the status register to be read by the microcontroller. Figure 3 shows this output, indicating the input power level.

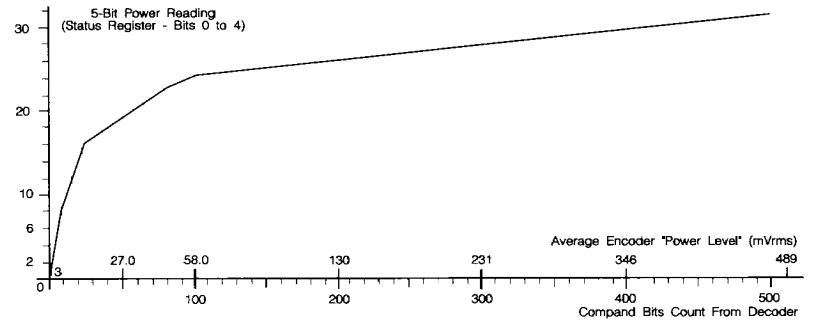



*Figure 3 - Compand (Power) Indications*

# Timing Information

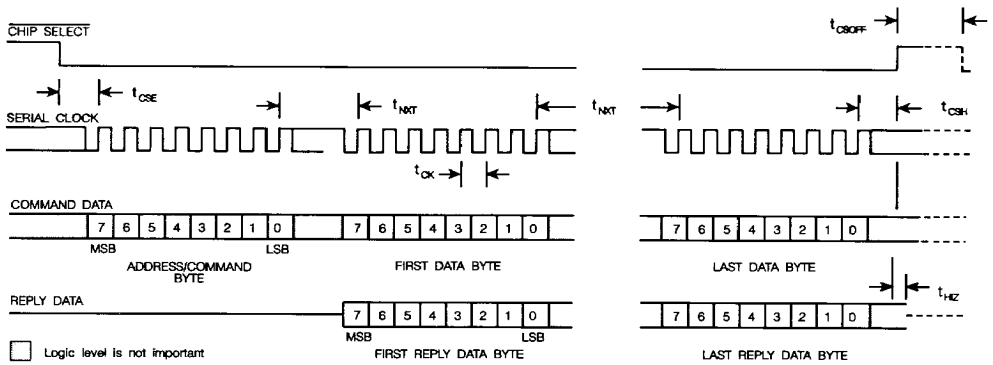



*Figure 4 - C-BUS Timing Information*

| Parameter - C-BUS Timing (Figure 4) | | Min. | | | Max. | Unit |
|---|---|---|---|---|---|---|
| | | a | b | c | | |
| $t_{CSE}$ | Chip Select Low to First Serial Clock Rising Edge | 2.0 | 4.0 | 8.0 | - | µs |
| $t_{CSH}$ | Last Serial Clock Rising Edge to Chip Select High | 4.0 | 4.0 | 8.0 | - | µs |
| $t_{HIZ}$ | Chip Select High to Reply Data High - Z | - | - | - | 2.0 | µs |
| $t_{CSOFF}$ | Chip Select High | 2.0 | 4.0 | 8.0 | - | µs |
| $t_{NXT}$ | Command Data Inter-Byte Time | 4.0 | 8.0 | 16.0 | - | µs |
| $t_{CK}$ | Serial Clock Period | 2.0 | 4.0 | 8.0 | - | µs |

| Parameter - Direct Address Timing (Figure 5) | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{CH}$ | Decoder or Encoder Clock High | 1.0 | - | - | µs |
| $t_{CL}$ | Decoder or Encoder Clock Low | 1.0 | - | - | µs |
| $t_{SU}$ | Decoder Data Set Up Time | .45 | - | - | µs |
| $t_{H}$ | Decoder Data Hold Time | .60 | - | - | µs |
| $t_{PCO}$ | Encoder Clock High to Encoder Data Valid | - | - | .75 | µs |
| $t_{SU}+t_{H}$ | Decoder Data True Time | | | | |

**Notes**

1. Minimum Timing Values
   (a) For all commands except "Read Data" and "Write Data" commands.
   (b) For "Read Data" and "Write Data" commands when *no* "Speech Store" or "Speech Play" commands are active.
   (c) For "Read Data" and "Write Data" commands when "Speech Store" or "Speech Play" commands are active.
2. Depending on the command, 1 or 2 bytes of Command Data are transmitted to the peripheral MSB (bit7) first, and LSB (bit0) last. Reply data is read from the peripheral MSB (bit7) first, and LSB (bit0) last.
3. To allow for different microcontroller serial interface formats, C-BUS compatible ICs are able to work with either polarity Serial Clock pulses.
4. Data is clocked into and out of the peripheral on the rising Serial Clock edge.
5. Loaded commands are acted upon at the end of each command.

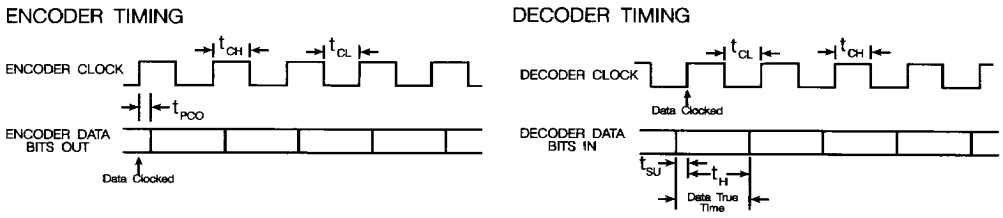



*Figure 5 - Codec Direct Access Timing*

# SPECIFICATIONS

## ABSOLUTE MAXIMUM RATINGS

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

| | |
|---|---|
| Supply Voltage | -0.3 to 7.0 V |
| Input Voltage at any pin (ref $V_{SS}$ = 0V) | -0.3 V to $V_{DD}$ + 0.3 V |
| Sink/Source Current (supply pins) | ±30mA |
| (other pins) | ±20mA |
| Total Device Dissipation @ $T_{AMB}$ = 25°C | 800mW max. |
| Derating | 10 mW/°C |
| Operating Temperature | -40°C to +85°C |
| Storage Temperature | -55°C to +125°C |

## OPERATING LIMITS

All devices were measured under the following conditions unless otherwise noted.

$V_{DD}$=5.0V

$T_{AMB}$=25°C

Xtal/Clock $f_0$ = 4.0MHz

Audio level 0dB ref. = 308 mVrms

Standard test signal $f_0$ = 820 Hz

Sample Rate = 31.25 kbit/s

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage ($V_{DD}$) | | 4.5 | 5.0 | 5.5 | V |
| Supply current (enabled) | 1 | - | 7.0 | - | mA |
| Supply current (powersave) | 1 | - | 1.0 | - | mA |
| **Digital Interface** | | | | | |
| Input Logic "1" | 2 | 3.5 | - | - | V |
| Input Logic "0" | 2 | - | - | 1.5 | V |
| Output Logic "1" | | | | | |
| at IOH = -120IA | 7 | 4.6 | - | - | V |
| at IOH = -500IA | 3 | 4.6 | - | - | V |
| Output Logic "0" | | | | | |
| at IOL = 360IA | 7,8 | - | - | 0.4 | V |
| at IOL = 500IA | 3 | - | - | 0.4 | V |
| Digital Input Current | | | | | |
| $V_{IN}$ = Logic "1" or "0" | 2 | - | - | 1.0 | µA |
| Leakage Current into $\overline{IRQ}$ "OFF" Output | 4 | - | - | 4.0 | µA |
| Digital Input Capacitance | 2 | - | - | 7.5 | pF |
| **Analog Impedance** | | | | | |
| Input Impedance | | - | 100 | - | kΩ |
| Output Impedance | | - | 1.5 | - | kΩ |
| **Dynamic Values** | | | | | |
| **Encoder** | | | | | |
| Analog Signal Input Levels | 5 | -24.0 | - | 4.0 | dB |
| Passband | | - | 3400 | - | Hz |
| **Decoder** | | | | | |
| Analog Signal Output Levels | 5 | -24.0 | - | 4.0 | dB |
| Passband | | 300 | - | 3400 | Hz |
| **Encoder/Decoder (Full Codec)** | | | | | |
| Passband | | 300 | - | 3400 | Hz |
| Passband Gain | | - | 0 | - | dB |
| Passband Ripple | | -3.0 | - | 3.0 | dB |
| Stopband | | 6.0 | - | 10 | kHz |
| Stopband Attenuation | | - | 50.0 | - | dB |
| SINAD Level | | - | 24.0 | - | dB |
| Output Noise (Input short circuit) | | - | -50 | - | dBp |
| Idle Channel Noise (Forced) | | - | -55 | - | dBp |
| Xtal/clock Frequency | 6 | - | 4.0 | - | MHz |

**Notes**

1. Does not include current drawn by any attached DRAM.
2. Serial Clock, Command Data, Chip Select, A1/DEI and A2/DCK inputs.
3. $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and A0 to A9 outputs.
4. When the $\overline{IRQ}$ outuput is at $V_{DD}$.
5. The optimum range of levels for a good Signal-to Noise ratio.
6. Audio frequency responses will vary with respect to Xtal/clock frequency.
7. Reply Data output.
8. $\overline{IRQ}$ output.