ML9208-xx

5 × 7 Dot Character × 16-Digit Display Controller/Driver with Character RAM

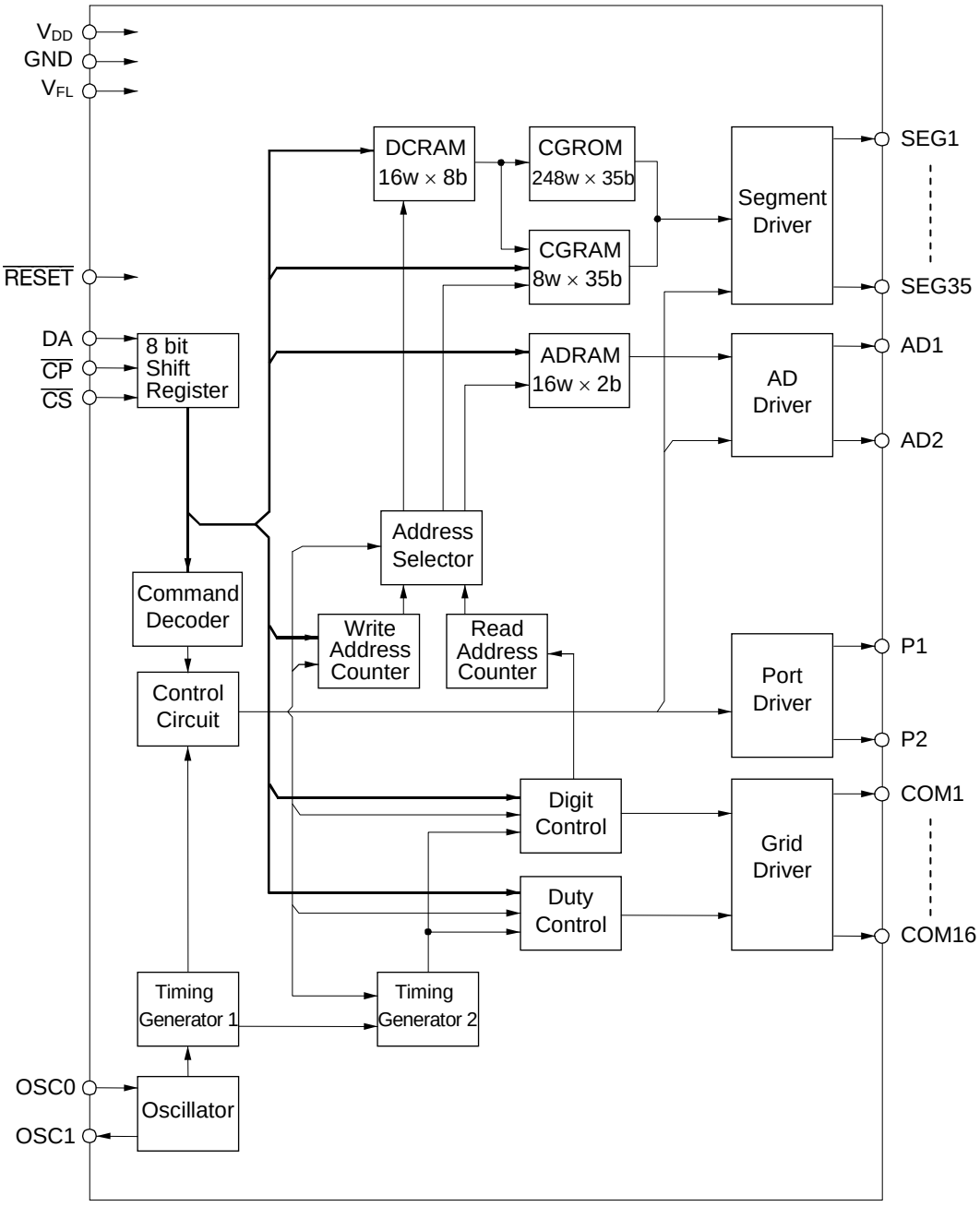
GENERAL DESCRIPTION

The ML9208-xx is a dot matrix vacuum fluorescent display tube controller driver IC which displays characters, numerics and symbols.
Dot matrix vacuum fluorescent display tube drive signals are generated by serial data sent from a micro-controller. A display system is easily realized by internal ROM and RAM for character display.

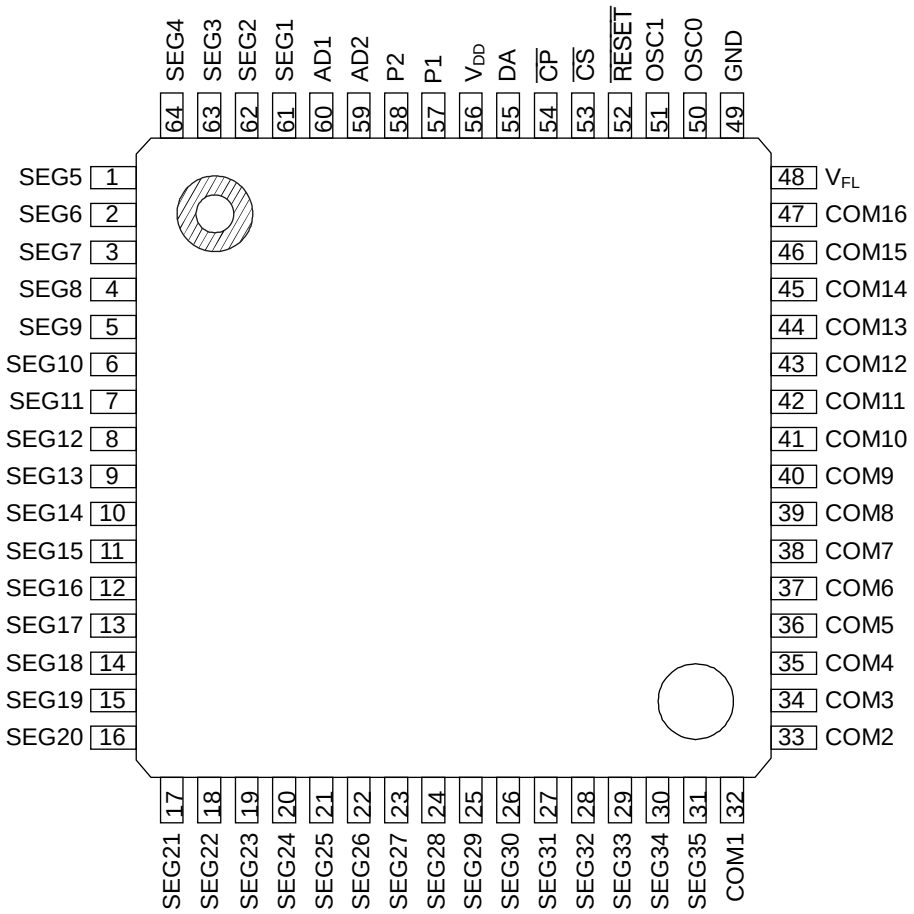
FEATURES

- Logic power supply and vacuum fluorescent display tube drive power supply (V_{DD})
  : 3.3 V ±10% or 5.0 V ±10%
- Fluorescent display tube drive power supply (V_{FL}) : V_{DD} –20 V to V_{DD} –42 V
- VFD driver output current
  (VFD driver output can be connected directly to the fluorescent display tube. No pull-down resistor is required.)
  - Segment driver (SEG1 to SEG35) : –6 mA (V_{FL} = V_{DD} –42 V)
  - Segment driver (AD1 and AD2) : –15 mA (V_{FL} = V_{DD} –42 V)
  - Grid driver (COM1 to COM16) : –30 mA (V_{FL} = V_{DD} –42 V)
- General output port output current
  - Output driver (P1 and P2) : ±1 mA (V_{DD} = 3.3 V ±10%)
    ±2 mA (V_{DD} = 5.0 V ±10%)
- Content of display
  - CGROM 5 × 7 dots : 248 types (character data)
  - CGRAM 5 × 7 dots : 8 types (character data)
  - ADRAM 16 (display digit) × 2 bits (symbol data)
  - DCRAM 16 (display digit) × 8 bits (register for character data display)
  - General output port 2 bits (static operation)
- Display control function
  - Display digit : 9 to 16 digits
  - Display duty (contrast adjustment) : 8 stages
  - All lights ON/OFFs
- 3 interfaces with microcontroller : DA, $\overline{CS}$, $\overline{CP}$ (4 interfaces when $\overline{RESET}$ is added)
- 1-byte instruction execution (excluding data write to RAM)
- Built-in oscillation circuit (external R and C)
- Package options:
  64-pin plastic QFP (QFP64-P-1414-0.80-BK) (ML9208-xxGA)
  64-pin plastic SSOP (SSOP64-P-525-0.80-K) (ML9208-xxMB)

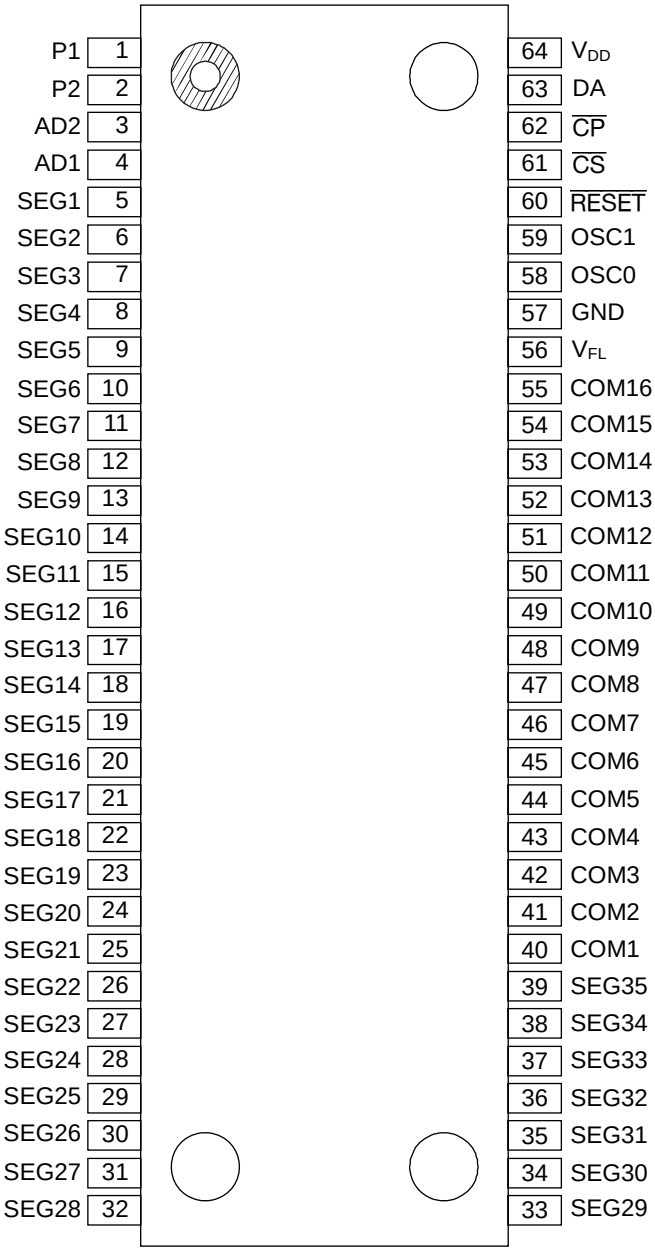
BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)

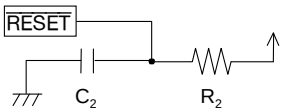
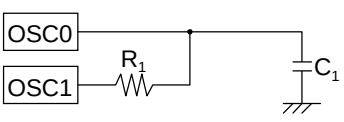


64-Pin Plastic QFP



64-Pin Plastic SSOP

PIN DESCRIPTION

Pin		Symbol	Type	Connects to	Description
QFP	SSOP				
1 to 31, 61 to 64	5 to 39	SEG1 to 35	O	Fluorescent tube anode electrode	Fluorescent display tube anode electrode drive output. Directly connected to fluorescent display tube and a pull-down resistor is not necessary. I_{OH} > –6 mA
32 to 47	40 to 55	COM1 to 16	O	Fluorescent tube grid electrode	Fluorescent display tube grid electrode drive output. Directly connected to fluorescent display tube and a pull-down resistor is not necessary. I_{OH} > –30 mA
59, 60	3, 4	AD1, AD2	O	Fluorescent tube anode electrode	Fluorescent display tube anode electrode drive output. Directly connected to fluorescent display tube and a pull-down resistor is not necessary. I_{OH} > –15 mA
57, 58	1, 2	P1, P2	O	LED drive control pins	General port output. Output of these pins in static operation, so these pins can drive the LED.
56	64	V_{DD}	—	Power supply	V_{DD}-GND are power supplies for internal logic. V_{DD}-V_{FL} are power supplies for driving fluorescent tubes. Apply V_{FL} after V_{DD} is applied.
49	57	GND			
48	56	V_{FL}			
55	63	DA	I	Microcontroller	Serial data input (positive logic). Input from LSB.
54	62	$\overline{CP}$	I	Microcontroller	Shift clock input. Serial data is shifted on the rising edge of $\overline{CP}$.
53	61	$\overline{CS}$	I	Microcontroller	Chip select input. Serial data transfer is disabled when $\overline{CS}$ pin is “H” level.
52	60	$\overline{RESET}$	I	Microcontroller or C_2, R_2	Reset input. “Low” initializes all the functions. Initial status is as follows. • Address of each RAM ···· address “00”H • Data of each RAM ····· Content is undefined • Display digit ····· 16 digits • Contrast adjustment ····· 8/16 • All lights ON or OFF ····· OFF mode • All outputs ····· “Low” level  (Circuit when R and C are connected externally) See Application Circuit.
50	58	OSC0	I	C_1, R_1	External RC pin for RC oscillation. Connect R and C externally. The RC time constant depends on the V_{DD} voltage used. Set the target oscillation frequency to 2 MHz.
51	59	OSC1	O		 (RC oscillation circuit) See Application Circuit.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition		Rating	Unit
Supply Voltage (1)	V_{DD}	—		–0.3 to 6.5	V
Supply Voltage (2)	V_{FL}	—		–45 to V_{DD} +0.3	V
Input Voltage	V_{IN}	—		–0.3 to V_{DD} +0.3	V
Power Dissipation	P_D	Ta ≥ 25°C	QFP	541	mW
			SSOP	590	
Storage Temperature	T_{STG}	—		–55 to 150	°C
Output Current	I_{O1}	COM1 to 16		–40 to 0.0	mA
	I_{O2}	AD1, AD2		–20 to 0.0	mA
	I_{O3}	SEG1 to 35		–10 to 0.0	mA
	I_{O4}	P1, P2		–4.0 to 4.0	mA

RECOMMENDED OPERATING CONDITIONS-1

When the power supply voltage is 5 V (typ.)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage (1)	V_{DD}	—	4.5	5.0	5.5	V
Supply Voltage (2)	V_{FL}	—	–36.5	—	–20	V
High Level Input Voltage	V_{IH}	All input pins excluding OSC0 pin	0.7 V_{DD}	—	—	V
Low Level Input Voltage	V_{IL}	All input pins excluding OSC0 pin	—	—	0.3 V_{DD}	V
$\overline{CP}$ Frequency	f_C	—	—	—	2.0	MHz
Oscillation Frequency	f_{OSC}	R_1 = 3.3 kΩ, C_1 = 39 pF	1.5	2.0	2.5	MHz
Frame Frequency	f_{FR}	DIGIT = 1 to 16, R_1 = 3.3 kΩ, C_1 = 39 pF	183	244	305	Hz
Operating Temperature	T_{op}	—	–40	—	85	°C

RECOMMENDED OPERATING CONDITIONS-2

When the power supply voltage is 3.3 V (typ.)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage (1)	V_{DD}	—	3.0	3.3	3.6	V
Supply Voltage (2)	V_{FL}	—	–38.4	—	–20	V
High Level Input Voltage	V_{IH}	All input pins excluding OSC0 pin	0.8 V_{DD}	—	—	V
Low Level Input Voltage	V_{IL}	All input pins excluding OSC0 pin	—	—	0.2 V_{DD}	V
$\overline{CP}$ Frequency	f_C	—	—	—	2.0	MHz
Oscillation Frequency	f_{OSC}	R_1 = 3.3 kΩ, C_1 = 39 pF	1.5	2.0	2.5	MHz
Frame Frequency	f_{FR}	DIGIT = 1 to 16, R_1 = 3.3 kΩ, C_1 = 39 pF	183	244	305	Hz
Operating Temperature	T_{op}	—	–40	—	85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics-1

(V_{DD} = 5.0 V ±10%, V_{FL} = V_{DD} –42 V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Applied pin	Condition	Min.	Max.	Unit
High Level Input Voltage	V_{IH}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	—	0.7 V_{DD}	—	V
Low Level Input Voltage	V_{IL}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	—	—	0.3 V_{DD}	V
High Level Input Current	I_{IH}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	V_{IH} = V_{DD}	–1.0	1.0	µA
Low Level Input Current	I_{IL}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	V_{IL} = 0.0 V	–1.0	1.0	µA
High Level Output Voltage	V_{OH1}	COM1 to 16	I_{OH1} = –30 mA	V_{DD} –1.5	—	V
	V_{OH2}	AD1, AD2	I_{OH2} = –15 mA	V_{DD} –1.5	—	V
	V_{OH3}	SEG1 to 35	I_{OH3} = –6 mA	V_{DD} –1.5	—	V
	V_{OH4}	P1, P2	I_{OH4} = –2 mA	V_{DD} –1.0	—	V
Low Level Output Voltage	V_{OL1}	COM1 to 16 AD1, AD2 SEG1 to 35	—	—	V_{FL} +1.0	V
	V_{OL2}	P1, P2	I_{OL1} = 2 mA	—	1.0	V
Current Consumption	I_{DD1}	V_{DD}	f_{OSC} = 2 MHz, no load Duty = 15/16 Digit = 1 to 16 All output lights ON	—	4	mA
	I_{DD2}	V_{DD}	f_{OSC} = 2 MHz, no load Duty = 8/16 Digit = 1 to 9 All output lights OFF	—	3	mA

DC Characteristics-2

(V_{DD} = 3.3 V ±10%, V_{FL} = V_{DD} –42 V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Applied pin	Condition		Min.	Max.	Unit
High Level Input Voltage	V_{IH}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	—		0.8 V_{DD}	—	V
Low Level Input Voltage	V_{IL}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	—		—	0.2 V_{DD}	V
High Level Input Current	I_{IH}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	V_{IH} = V_{DD}		–1.0	1.0	µA
Low Level Input Current	I_{IL}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	V_{IL} = 0.0 V		–1.0	1.0	µA
High Level Output Voltage	V_{OH1}	COM1 to 16	I_{OH1} = –30 mA		V_{DD} –1.5	—	V
	V_{OH2}	AD1, AD2	I_{OH2} = –15 mA		V_{DD} –1.5	—	V
	V_{OH3}	SEG1 to 35	I_{OH3} = –6 mA		V_{DD} –1.5	—	V
	V_{OH4}	P1, P2	I_{OH4} = –1 mA		V_{DD} –1.0	—	V
Low Level Output Voltage	V_{OL1}	COM1 to 16 AD1, AD2 SEG1 to 35	—		—	V_{FL} +1.0	V
	V_{OL2}	P1, P2	I_{OL1} = 1 mA		—	1.0	V
Current Consumption	I_{DD1}	V_{DD}	F_{OSC} = 2 MHz, no load	Duty = 15/16 Digit = 1 to 16 All output lights ON	—	3	mA
	I_{DD2}			Duty = 8/16 Digit = 1 to 9 All output lights OFF	—	2	mA

AC Characteristics-1

(V_{DD} = 5.0 V ±10%, V_{FL} = V_{DD} –42 V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Max.	Unit
$\overline{CP}$ Frequency	f_C	—		—	2.0	MHz
$\overline{CP}$ Pulse Width	t_{CW}	—		250	—	ns
DA Setup Time	t_{DS}	—		250	—	ns
DA Hold Time	t_{DH}	—		250	—	ns
$\overline{CS}$ Setup Time	t_{CSS}	—		250	—	ns
$\overline{CS}$ Hold Time	t_{CSH}	R_1 = 3.3 kΩ, C_1 = 39 pF		16	—	µs
$\overline{CS}$ Wait Time	t_{CSW}	—		250	—	ns
Data Processing Time	t_{DOFF}	R_1 = 3.3 kΩ, C_1 = 39 pF		8	—	µs
$\overline{RESET}$ Pulse Width	t_{WRES}	When $\overline{RESET}$ signal is input from microcontroller etc. externally		250	—	ns
$\overline{RESET}$ Time	t_{RSON}	When $\overline{RESET}$ signal is input from microcontroller etc. externally		250	—	ns
		R_2 = 1.0 kΩ, C_2 = 0.1 µF		—	200	µs
DA Wait Time	t_{RSOFF}	—		250	—	ns
All Output Slew Rate	t_R	C_l = 100 pF	t_R = 20 to 80%	—	2.0	µs
	t_F		t_F = 80 to 20%	—	2.0	µs
V_{DD} Rise Time	t_{PRZ}	When mounted in the unit		—	100	µs
V_{DD} Off Time	t_{POF}	When mounted in the unit, V_{DD} = 0.0 V		5.0	—	ms

AC Characteristics-2

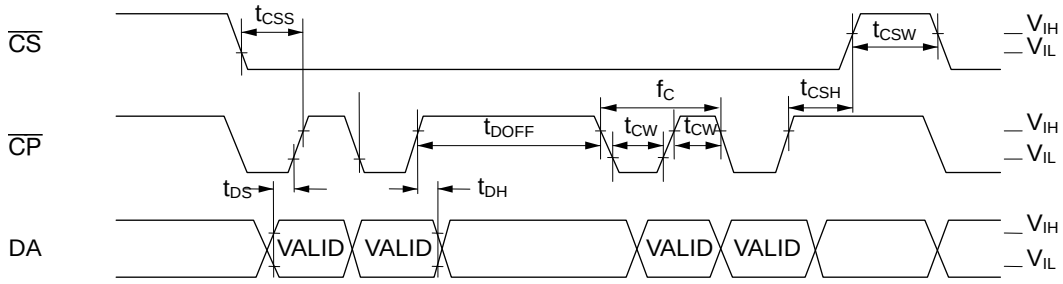
(V_{DD} = 3.3 V ±10%, V_{FL} = V_{DD} –42 V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Max.	Unit
$\overline{CP}$ Frequency	f_C	—		—	2.0	MHz
$\overline{CP}$ Pulse Width	t_{CW}	—		250	—	ns
DA Setup Time	t_{DS}	—		250	—	ns
DA Hold Time	t_{DH}	—		250	—	ns
$\overline{CS}$ Setup Time	t_{CSS}	—		250	—	ns
$\overline{CS}$ Hold Time	t_{CSH}	R_1 = 3.3 kΩ, C_1 = 39 pF		16	—	µs
$\overline{CS}$ Wait Time	t_{CSW}	—		250	—	ns
Data Processing Time	t_{DOFF}	R_1 = 3.3 kΩ, C_1 = 39 pF		8	—	µs
$\overline{RESET}$ Pulse Width	t_{WRES}	When $\overline{RESET}$ signal is input from microcontroller etc. externally		250	—	ns
$\overline{RESET}$ Time	t_{RSON}	When $\overline{RESET}$ signal is input from microcontroller etc. externally		250	—	ns
		R_2 = 1.0 kΩ, C_2 = 0.1 µF		—	200	µs
DA Wait Time	t_{RSOFF}	—		250	—	ns
All Output Slew Rate	t_R	C_l = 100 pF	t_R = 20 to 80%	—	2.0	µs
	t_F		t_F = 80 to 20%	—	2.0	µs
V_{DD} Rise Time	t_{PRZ}	When mounted in the unit		—	100	µs
V_{DD} Off Time	t_{POF}	When mounted in the unit, V_{DD} = 0.0 V		5.0	—	ms

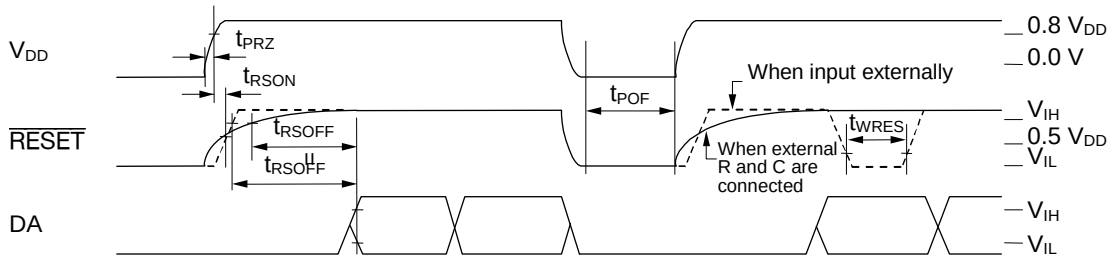
TIMING DIAGRAM

Symbol	V_{DD} = 3.3 V ±10%	V_{DD} = 5.0 V ±10%
V_{IH}	0.8 V_{DD}	0.7 V_{DD}
V_{IL}	0.2 V_{DD}	0.3 V_{DD}

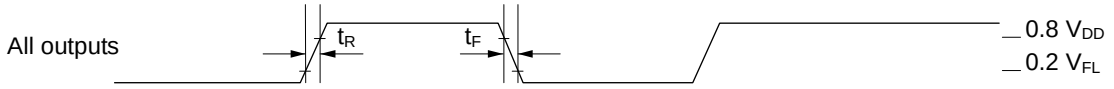
• Data Timing



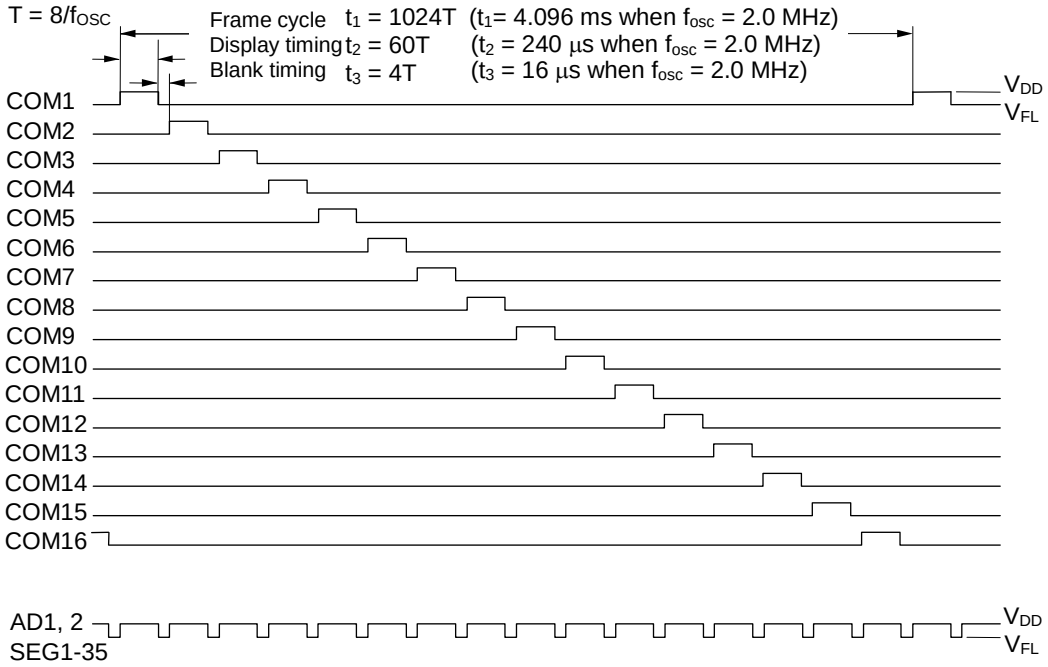
• Reset Timing



• Output Timing



• **Digit Output Timing (for 16-digit display, at a duty of 15/16)**



FUNCTIONAL DESCRIPTION

Commands List

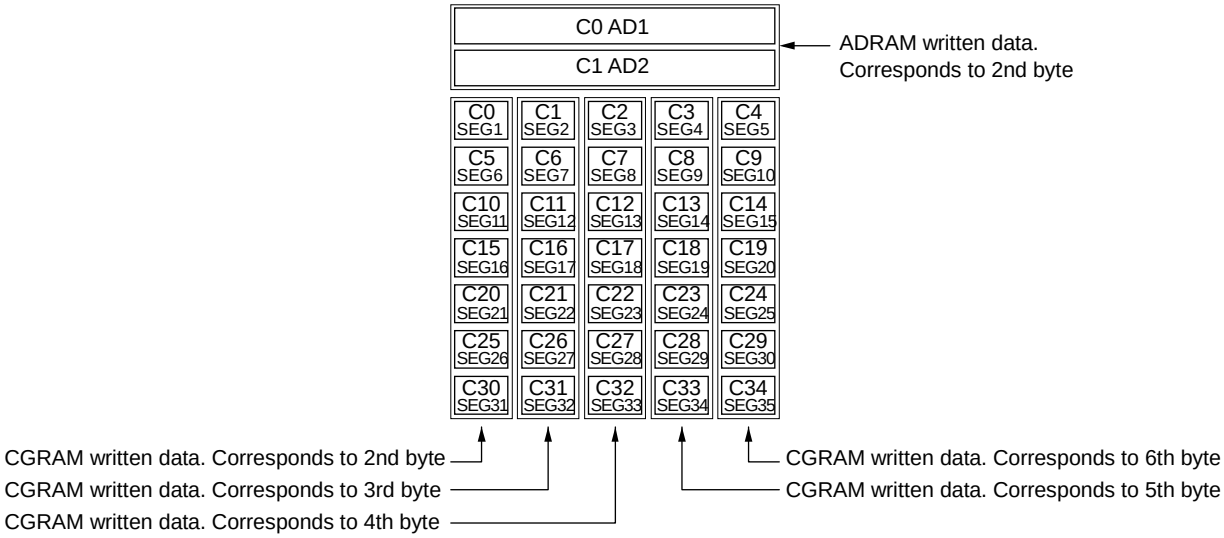
	Command	LSB 1st byte							MSB	LSB 2nd byte							MSB	
		B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	
1	DCRAM data write	X0	X1	X2	X3	1	0	0	0	C0	C1	C2	C3	C4	C5	C6	C7	
2	CGRAM data write	X0	X1	X2	*	0	1	0	0	C0	C5	C10	C15	C20	C25	C30	*	2nd byte
										C1	C6	C11	C16	C21	C26	C31	*	3rd byte
										C2	C7	C12	C17	C22	C27	C32	*	4th byte
										C3	C8	C13	C18	C23	C28	C33	*	5th byte
										C4	C9	C14	C19	C24	C29	C34	*	6th byte
3	ADRAM data write	X0	X1	X2	X3	1	1	0	0	C0	C1	*	*	*	*	*	*	
4	General output port set	P1	P2	*	*	0	0	1	0									
5	Display duty set	D0	D1	D2	*	1	0	1	0									
6	Number of digits set	K0	K1	K2	*	0	1	1	0									
7	All lights ON/OFF	L	H	*	*	1	1	1	0									
	Test mode																	

*: Don't care
Xn: Address specification for each RAM
Cn: Character code specification for each RAM
Pn: General output port status specification
Dn: Display duty specification
Kn: Number of digits specification
H: All lights ON instruction
L: All lights OFF instruction

When data is written to RAM (DCRAM, CGRAM, ADRAM) continuously, addresses are internally incremented automatically.
Therefore it is not necessary to specify the 1st byte to write RAM data for the 2nd and later bytes.

Note: The test mode is used for inspection before shipment. It is not a user function.

Positional Relationship Between SEGn and ADn (one digit)

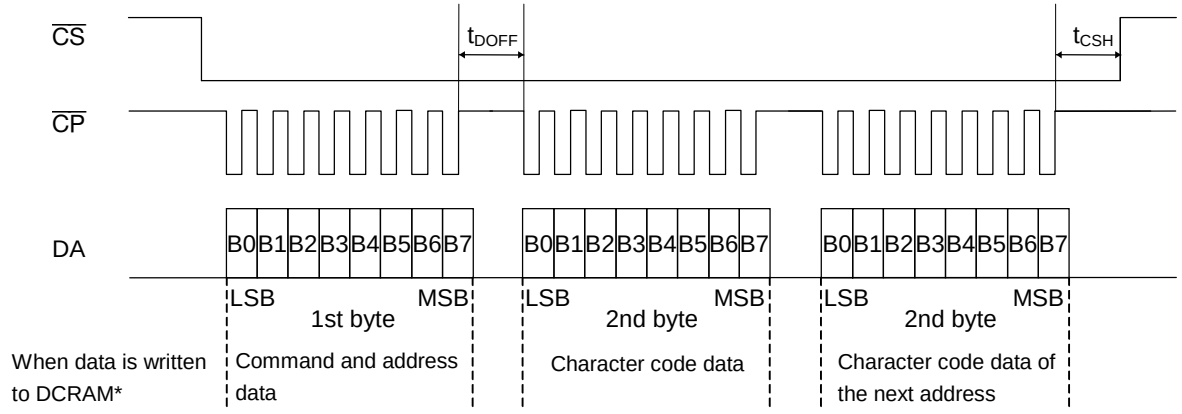


Data Transfer Method and Command Write Method

Display control command and data are written by an 8-bit serial transfer.
Write timing is shown in the figure below.

Setting the $\overline{CS}$ pin to "Low" level enables a data transfer.
Data is 8 bits and is sequentially input into the DA pin from LSB (LSB first).
As shown in the figure below, data is read by the shift register at the rising edge of the shift clock, which is input into the $\overline{CP}$ pin. If 8-bit data is input, internal load signals are automatically generated and data is written to each register and RAM.
Therefore it is not necessary to input load signals from the outside.

Setting the $\overline{CS}$ pin to "High" disables data transfer. Data input from the point when the $\overline{CS}$ pin changes from "High" to "Low" is recognized in 8-bit units.



* When data is written to RAM (DCRAM, ADRAM, CGRAM) continuously, addresses are internally incremented automatically.
Therefore it is not necessary to specify the 1st byte to write RAM data for the 2nd and later bytes.

Reset Function

Reset is executed when the $\overline{RESET}$ pin is set to "L", (when turning power on, for example) and initializes all functions.
Initial status is as follows.

- Address of each RAM ····· address "00"H
- Data of each RAM ····· All contents are undefined
- General output port ····· All general output ports go "Low"
- Display digit ····· 16 digits
- Contrast adjustment ····· 8/16
- All display lights ON or OFF ···· OFF mode
- Segment output ····· All segment outputs go "Low"
- AD output ····· All AD outputs go "Low"

Please set again according to "Setting Flowchart" after reset.

Description of Commands and Functions

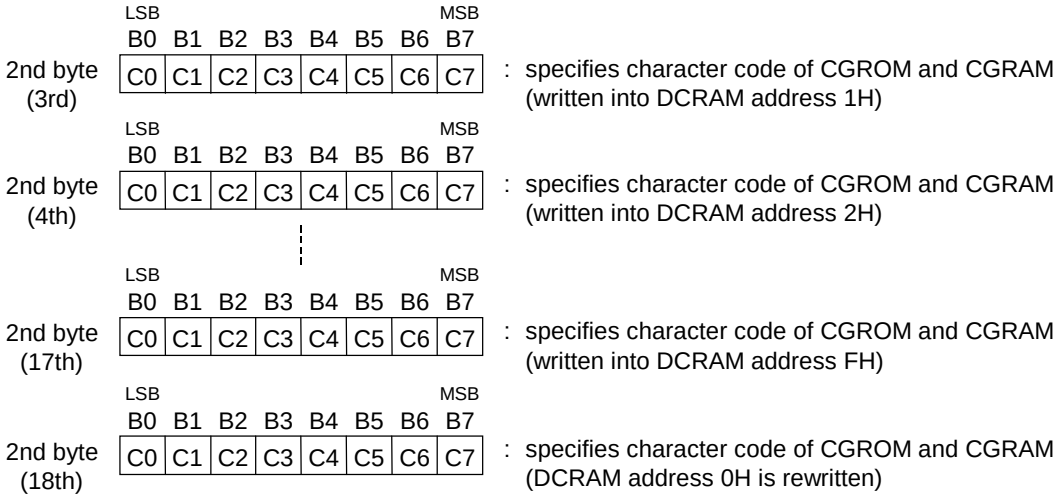
1. DCRAM data write
   (Specifies the address of DCRAM and writes the character code of CGROM and CGRAM.)

DCRAM (Data Control RAM) has a 4-bit address to store character code of CGROM and CGRAM.
The character code specified by DCRAM is converted to a 5 × 7 dot matrix character pattern via CGROM or CGRAM.
(The DCRAM can store 16 characters.)

[Command format]

	LSB							MSB		
	B0	B1	B2	B3	B4	B5	B6	B7		
1st byte (1st)	X0	X1	X2	X3	1	0	0	0	:	selects DCRAM data write mode and specifies DCRAM address (Ex: Specifies DCRAM address 0H)
	LSB							MSB		
	B0	B1	B2	B3	B4	B5	B6	B7		
2nd byte (2nd)	C0	C1	C2	C3	C4	C5	C6	C7	:	specifies character code of CGROM and CGRAM (written into DCRAM address 0H)

To specify the character code of CGROM and CGRAM continuously to the next address, specify only character code as follows.
The addresses of DCRAM are automatically incremented. Specification of an address is unnecessary.



X0 (LSB) to X3 (MSB) : DCRAM addresses (4 bits: 16 characters)

C0 (LSB) to C7 (MSB) : Character code of CGROM and CGRAM (8 bits: 256 characters)

[COM positions and set DCRAM addresses]

HEX	X0	X1	X2	X3	COM position
0	0	0	0	0	COM1
1	1	0	0	0	COM2
2	0	1	0	0	COM3
3	1	1	1	0	COM4
4	0	0	1	0	COM5
5	1	0	1	0	COM6
6	0	1	1	0	COM7
7	1	1	1	0	COM8
8	0	0	0	1	COM9
9	1	0	0	1	COM10
A	0	1	0	1	COM11
B	1	1	0	1	COM12
C	0	0	1	1	COM13
D	1	0	1	1	COM14
E	0	1	1	1	COM15
F	1	1	1	1	COM16

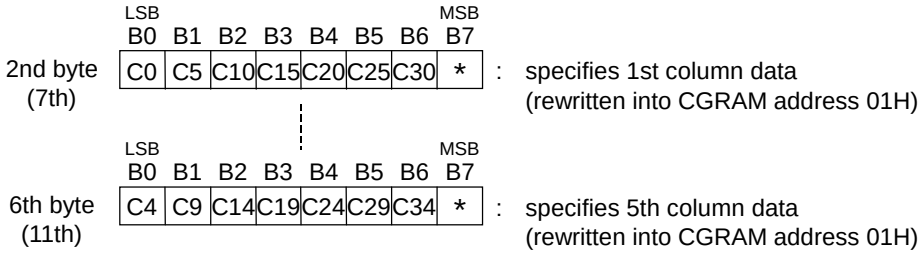
2. CGRAM data write
   (Specifies the addresses of CGRAM and writes character pattern data.)

   CGRAM (Character Generator RAM) has a 3-bit address to store 5 × 7 dot matrix character patterns.
   A character pattern stored in CGRAM can be displayed by specifying the character code (address) by DCRAM.
   The address of CGRAM is assigned to 00H to 07H. (All the other addresses are the CGROM addresses.)
   (The CGRAM can store 8 types of character patterns.)

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7		
1st byte (1st)	X0	X1	X2	*	0	1	0	0	:	selects CGRAM data write mode and specifies CGRAM address. (Ex: specifies CGRAM address 00H)
2nd byte (2nd)	C0	C5	C10	C15	C20	C25	C30	*	:	specifies 1st column data (rewritten into CGRAM address 00H)
3rd byte (3rd)	C1	C6	C11	C16	C21	C26	C31	*	:	specifies 2nd column data (rewritten into CGRAM address 00H)
4th byte (4th)	C2	C7	C12	C17	C22	C27	C32	*	:	specifies 3rd column data (rewritten into CGRAM address 00H)
5th byte (5th)	C3	C8	C13	C18	C23	C28	C33	*	:	specifies 4th column data (rewritten into CGRAM address 00H)
6th byte (6th)	C4	C9	C14	C19	C24	C29	C34	*	:	specifies 5th column data (rewritten into CGRAM address 00H)

   To specify character pattern data continuously to the next address, specify only character pattern data as follows.
   The addresses of CGRAM are automatically incremented. Specification of an address is therefore unnecessary.
   The 2nd to 6th byte (character pattern data) are regarded as one data item, so 250 ns is sufficient for t_{DOFF} time between bytes.



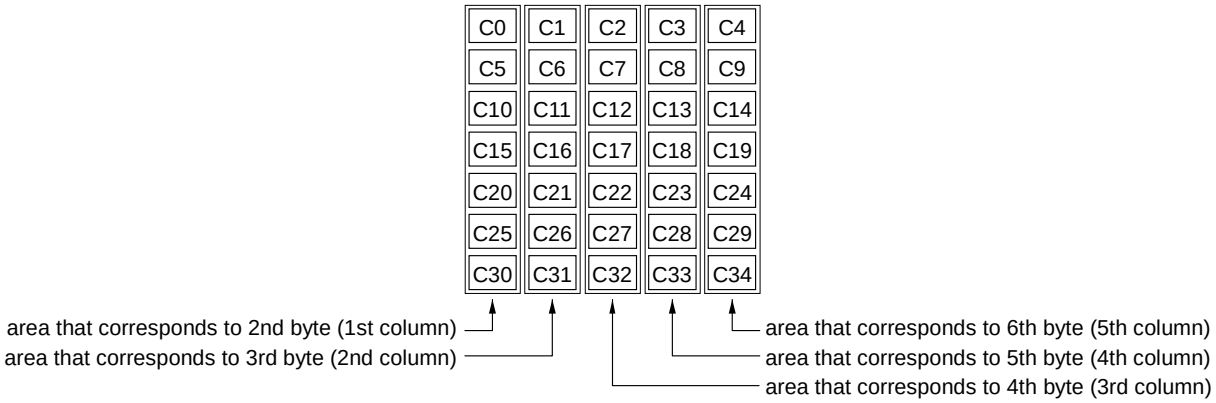
X0 (LSB) to X2 (MSB) : CGRAM addresses (3 bits: 8 characters)
C0 (LSB) to C34 (MSB) : Character pattern data (35 bits: 35 outputs per digit)
* : Don't care

[CGROM addresses and set CGRAM addresses]

Refer to ROMCODE table

HEX	X0	X1	X2	CGROM address
00	0	0	0	RAM00(00000000B)
01	1	0	0	RAM01(00000001B)
02	0	1	0	RAM02(00000010B)
03	1	1	0	RAM03(00000011B)
04	0	0	1	RAM04(00000100B)
05	1	0	1	RAM05(00000101B)
06	0	1	1	RAM06(00000110B)
07	1	1	1	RAM07(00000111B)

Positional relationship between the output area of CGROM and that of CGRAM

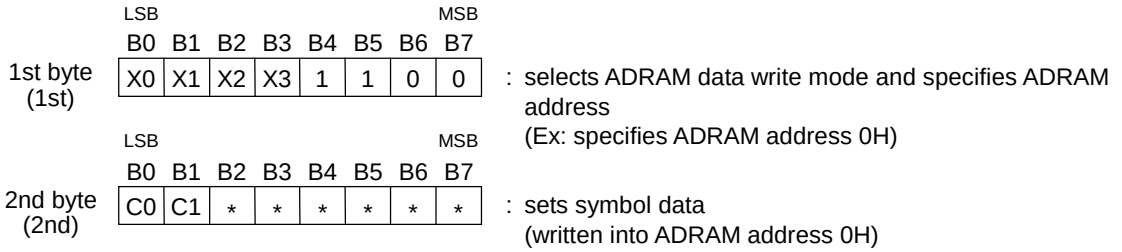


Note: CGROM (Character Generator ROM) has an 8-bit address to generate 5 × 7 dot matrix character patterns. CGRAM can store 248 types of character patterns.

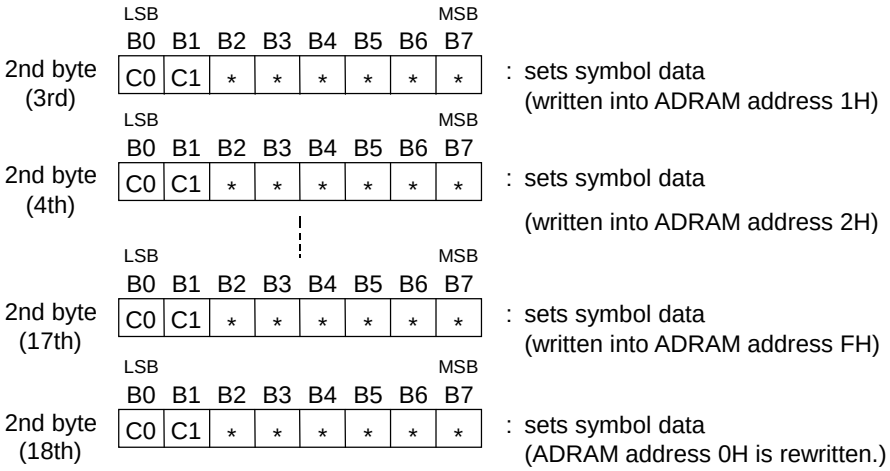
3. ADRAM data write
   (specifies address of ADRAM and writes symbol data)

   ADRAM (Additional Data RAM) has a 2-bit address to store symbol data.
   Symbol data specified by ADRAM is directly output without CGROM and CGRAM.
   (The ADRAM can store 2 types of symbol patterns for each digit.)
   The terminal to which the contents of ADRAM are output can be used as a cursor.

[Command format]



To specify symbol data continuously to the next address, specify only symbol data as follows.
The address of ADRAM is automatically incremented. Specification of addresses is therefore unnecessary.



X0 (LSB) to X3 (MSB) : ADRAM addresses (4 bits: 16 characters)
C0 (LSB) to C1 (MSB) : Symbol data (2 bits: 2-symbol data per digit)
* : Don't care

[COM positions and ADRAM addresses]

HEX	X0	X1	X2	X3	COM position
0	0	0	0	0	COM1
1	1	0	0	0	COM2
2	0	1	0	0	COM3
3	1	1	1	0	COM4
4	0	0	1	0	COM5
5	1	0	1	0	COM6
6	0	1	1	0	COM7
7	1	1	1	0	COM8
8	0	0	0	1	COM9
9	1	0	0	1	COM10
A	0	1	0	1	COM11
B	1	1	0	1	COM12
C	0	0	1	1	COM13
D	1	0	1	1	COM14
E	0	1	1	1	COM15
F	1	1	1	1	COM16

4. General output port set
(specifies the general output port status)

The general output port is an output for 2-bit static operation.
It is used to control other I/O devices and turn on LED. (static operation)
When at the "High" level, this output becomes the V_{DD} voltage, and when at the "Low" level, it becomes the ground potential. Therefore, the fluorescent display tube cannot be driven.

[Command format]

	LSB							MSB	
	B0	B1	B2	B3	B4	B5	B6	B7	
1st byte	P1	P2	*	*	0	0	1	0	: selects a general output port and specifies the output status

P1, P2 : general output port
* : don't care

[Set data and set state of general output port]

P1	P2	Display state of general output port	
0	0	Sets P1 and P2 to low	← (The state when power is applied or when $\overline{\text{RESET}}$ is input.)
1	0	Sets P1 to high and P2 to low	
0	1	Sets P1 to low and P2 to high	
1	1	Sets P1 and P2 to high	

5. Display duty set
   (writes display duty value to duty cycle register)

   Display duty adjusts contrast in 8 stages using 3-bit data.
   When power is turned on or when the $\overline{\text{RESET}}$ signal is input, the duty cycle register value is "0". Always execute this instruction before turning the display on, then set a desired duty value.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	D0	D1	D2	*	1	0	1	0	: selects display duty set mode and sets duty value

D0 (LSB) to D2 (MSB) : display duty data (3 bits: 8 stages)
* : don't care

[Relation between setup data and controlled COM duty]

HEX	D0	D1	D2	COM duty	
0	0	0	0	8/16	← (The state when power is turned on or when $\overline{\text{RESET}}$ signal is input.)
1	1	0	0	9/16	
2	0	1	0	10/16	
3	1	1	0	11/16	
4	0	0	1	12/16	
5	1	0	1	13/16	
6	0	1	1	14/16	
7	1	1	1	15/16	

6. Number of digits set
(writes the number of display digits to the display digit register)

The number of digits set can display 9 to 16 digits using 3-bit data.
When power is turned on or when a $\overline{\text{RESET}}$ signal is input, the number of digit register value is "0". Always execute this instruction to change the number of digits before turning the dispaly on.

[Command format]

	LSB							MSB	
	B0	B1	B2	B3	B4	B5	B6	B7	
1st byte	K0	K1	K2	*	0	1	1	0	: selects the number of digit set mode and specifies the number of digit value

K0 (LSB) to K2 (MSB) : number of digit data (3 bits: 8 digits)
* : don't care

[Relation between setup data and controlled COM]

HEX	K0	K1	K2	Number of digits of COM	
0	0	0	0	COM1 to 16	← (The state when power is turned on or when $\overline{\text{RESET}}$ signal is input.)
1	1	0	0	COM1 to 9	
2	0	1	0	COM1 to 10	
3	1	1	0	COM1 to 11	
4	0	0	1	COM1 to 12	
5	1	0	1	COM1 to 13	
6	0	1	1	COM1 to 14	
7	1	1	1	COM1 to 15	

7. All display lights ON/OFF set
   (turns all dispaly lights ON or OFF)

   All display lights ON is used primarily for display testing.
   All display lights OFF is primarily used for display blink and to prevent malfunction when power is turned on.
   This command cannot control the general output port.

[Command format]

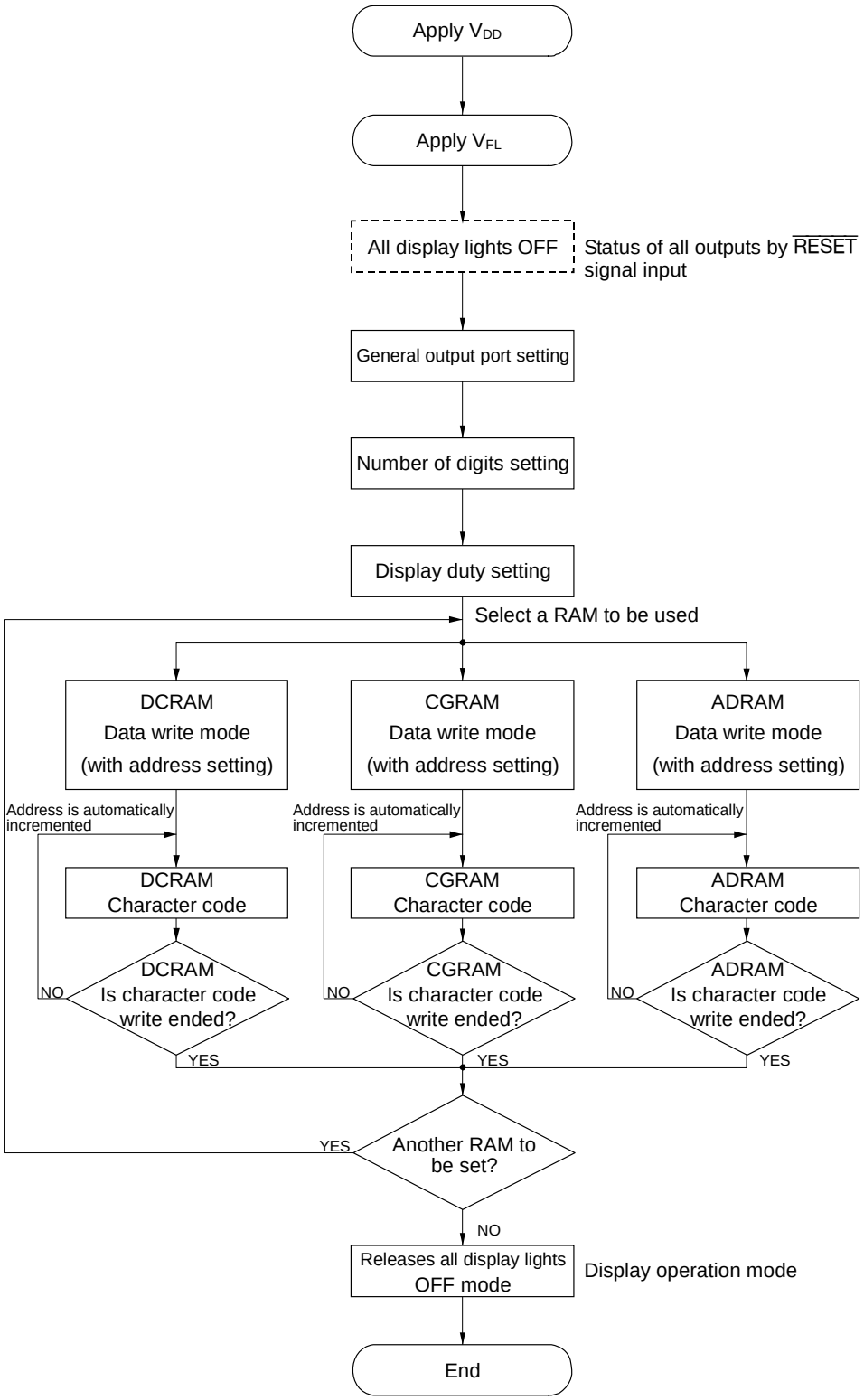
	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	L	H	*	*	1	1	1	0	: selects all display lights ON or OFF mode

L: sets all lights OFF
H: sets all lights ON
*: Don't care

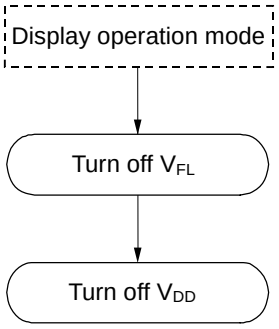
[Set data and display state of SEG and AD]

L	H	Display state of SEG and AD	
0	0	Normal display	
1	0	Sets all outputs to Low	← (The state when power is applied or when $\overline{\text{RESET}}$ is input.)
0	1	Sets all outputs to High	
1	1	Sets all outputs to High	← (All lights ON mode has priority.)

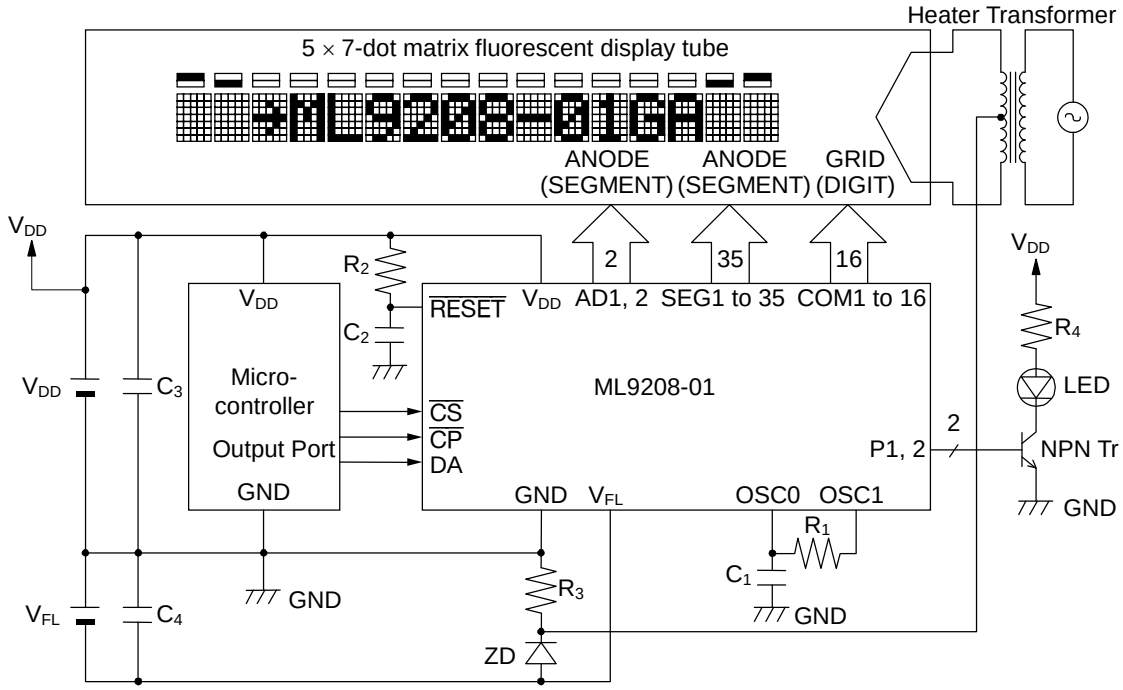
Setting Flowchart
(Power applying included)



Power-off Flowchart



APPLICATION CIRCUIT

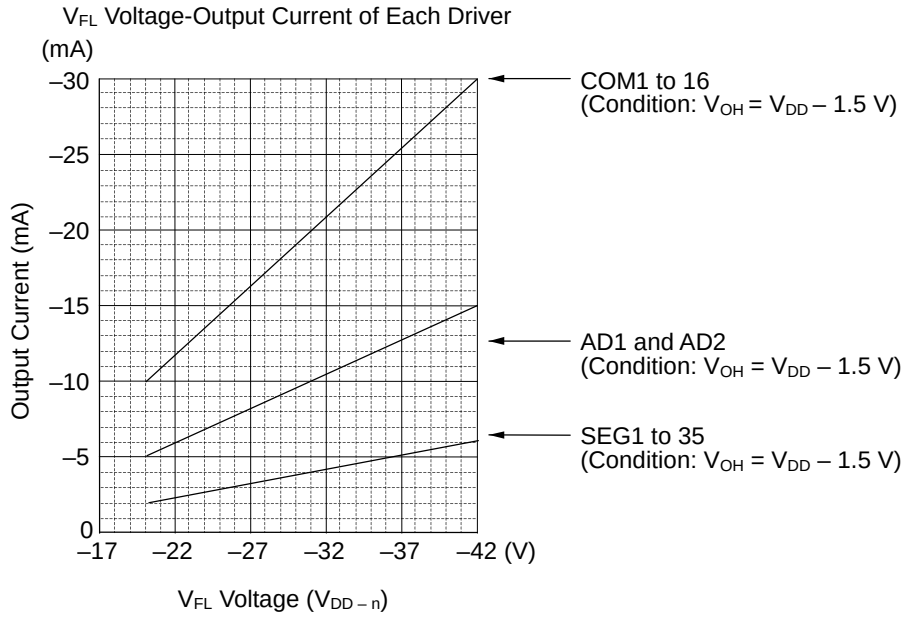


Notes: 1. The V_{DD} value depends on the power supply voltage of the microcontroller used. Adjust the values of the constants R_1, R_2, R_4, C_1, and C_2 to the power supply voltage used.

2. The V_{FL} value depends on the fluorescent display tube used. Adjust the values of the constants R_3 and ZD to the power supply voltage used.

Reference data

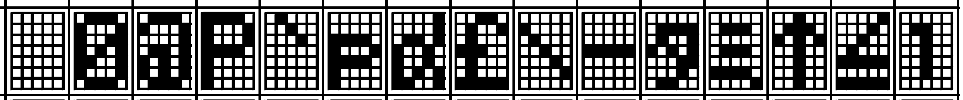
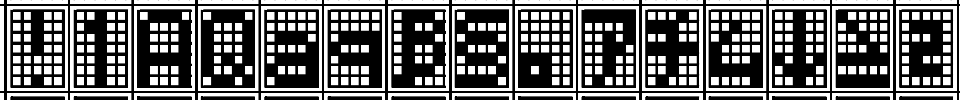
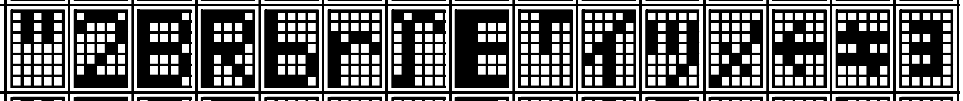
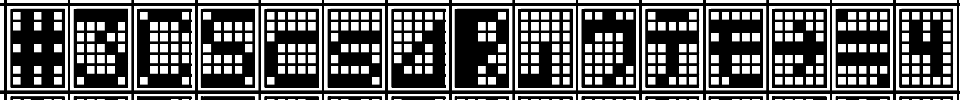
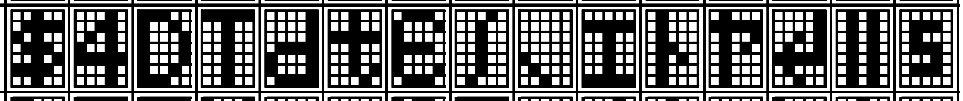
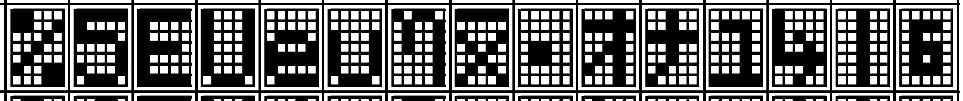
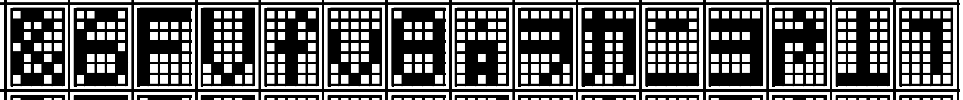
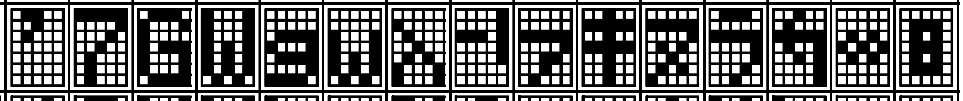
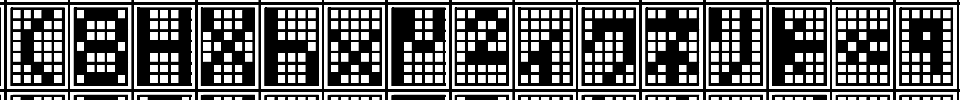
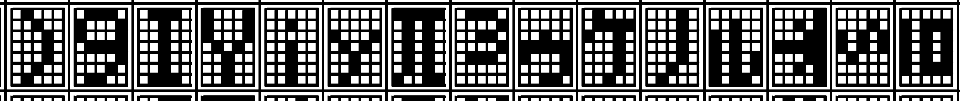
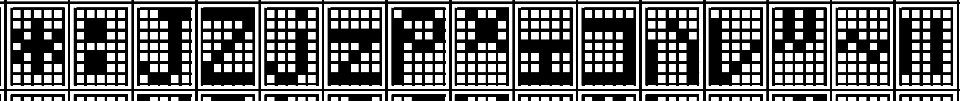
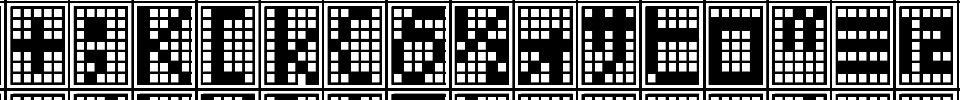
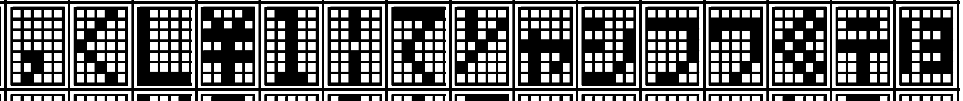
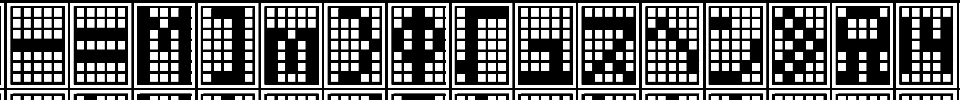
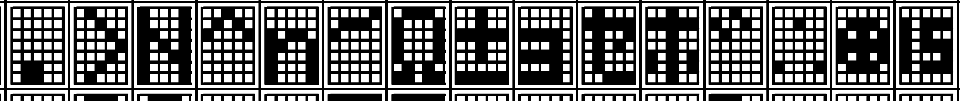
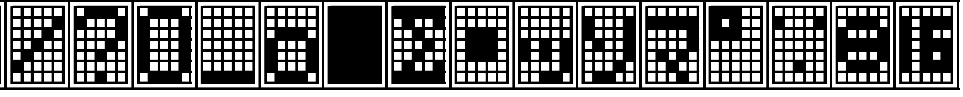
The figure below shows the relationship between the V_{FL} voltage and the output current of each driver. Take care that the total power consumption to be used does not exceed the power dissipation.



ML9208-01 ROM CODE

* ROM CODE_A is the character set for SEGA1 to SEGA35.

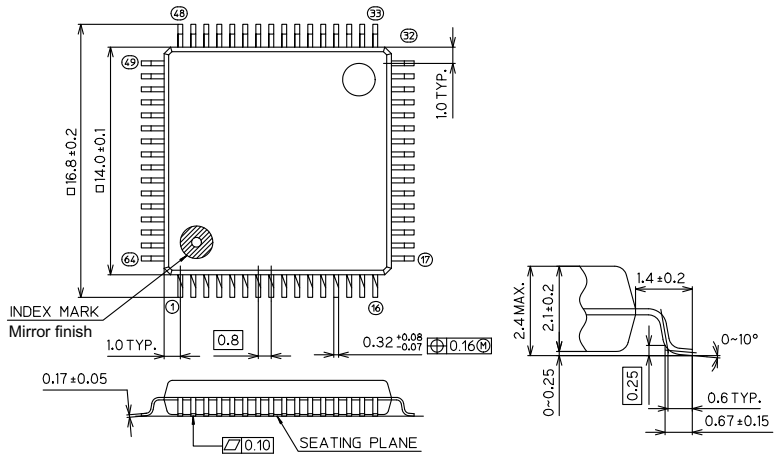
*00000000b(00h) to 00001111b(0Fh) are the CGRAM_A addresses.

MSB / LSB	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	RAM0															
0001	RAM1															
0010	RAM2															
0011	RAM3															
0100	RAM4															
0101	RAM5															
0110	RAM6															
0111	RAM7															
1000																
1001																
1010																
1011																
1100																
1101																
1110																
1111																

PACKAGE DIMENSIONS

(Unit: mm)

QFP64-P-1414-0.80-BK



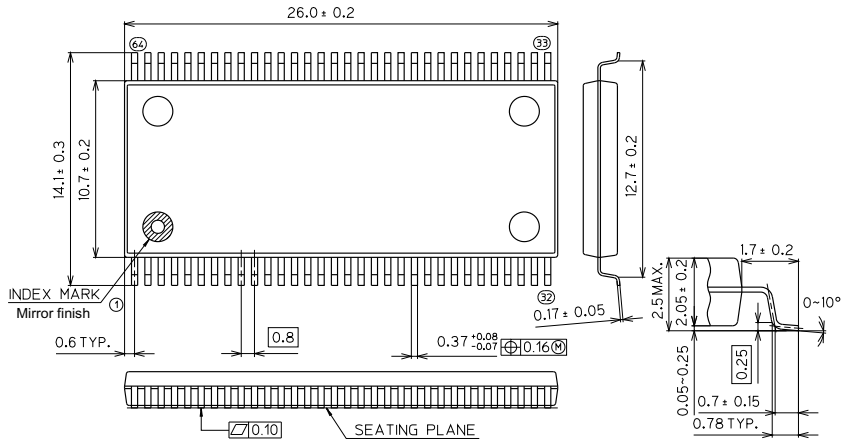
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.87 TYP.
Rev. No./Last Revised	6/Feb. 23, 2001

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit: mm)

SSOP64-P-525-0.80-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	1.34 TYP.
Rev. No./Last Revised	3/Dec. 5, 1996

Notes for Mounting the Surface Mount Type Package

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REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL9208-01	Oct. 23, 2003	–	–	Final edition 1
FEDL9208-02	Nov. 16, 2009	9	9	47pF→39 pF

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