LH540215/25

512 × 18 / 1024 × 18 Synchronous FIFO

FEATURES

- Fast Cycle Times: 20/25/35 ns
- Pin-Compatible Drop-In Replacements for IDT72215B/25B FIFOs
- Choice of IDT-Compatible or ***Enhanced*** Operating Mode; Selected by an Input Control Signal
- Device Comes Up into One of Two Known Default States at Reset Depending on the State of the ***EMODE*** Control Input: Programming is Allowed, but is not Required
- Internal Memory Array Architecture Based on CMOS Dual-Port SRAM Technology, 512 × 18 or 1024 × 18
- 'Synchronous' Enable-Plus-Clock Control at Both Input Port and Output Port
- Independently-Synchronized Operation of Input Port and Output Port
- Control Inputs Sampled on Rising Clock Edge
- Most Control Signals Assertive-LOW for Noise Immunity
- May be Cascaded for Increased Depth, or Paralleled for Increased Width
- Five Status Flags: Full, Almost-Full, Half-Full, Almost-Empty, and Empty; 'Almost' Flags are Programmable
- ***In Enhanced Operating Mode, Almost-Full, Half-Full, and Almost-Empty Flags can be Made Completely Synchronous***
- ***In Enhanced Operating Mode, Duplicate Enables for Interlocked Paralleled FIFO Operation, for 36-Bit Data Width, when Selected and Appropriately Connected***
- ***In Enhanced Operating Mode, Disabling Three-State Outputs May be Made to Suppress Reading***
- ***Data Retransmit Function***
- TTL/CMOS-Compatible I/O
- Space-Saving 68-Pin PLCC Package, and 64-Pin TQFP Package

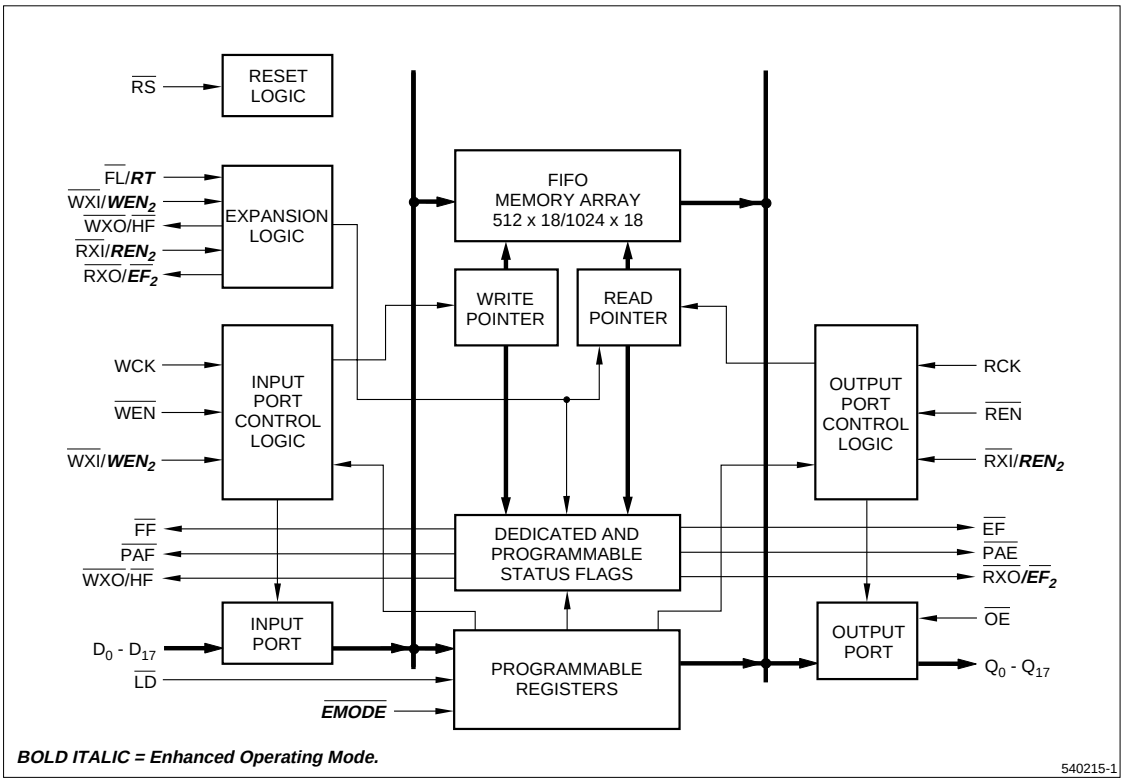


Figure 1. LH540215/25 Block Diagram

BOLD ITALIC = Enhanced Operating Mode

FUNCTIONAL DESCRIPTION

NOTE: Throughout this data sheet, a ***BOLD ITALIC*** type font is used for all references to ***Enhanced Operating Mode*** features which do not function in IDT-Compatible Operating Mode; and also for all references to the ***retransmit*** facility (which is not an IDT72215B/25B FIFO feature), even though it may be used – subject to some restrictions – in either of these two operating modes. Thus, readers interested only in using the LH540215/25 FIFOs in IDT-Compatible Operating Mode may skip over ***BOLD ITALIC*** sections, if they wish.

The LH540215/25 parts are FIFO (First-In, First-Out) memory devices, based on fully-static CMOS dual-port SRAM technology, capable of containing up to 512 or 1024 18-bit words respectively. They can replace two or more byte-wide FIFOs in many applications, for microprocessor-to-microprocessor or microprocessor-to-bus communication. Their architecture supports synchronous operation, tied to two independent free-running clocks at the input and output ports respectively. However, these 'clocks' also may be aperiodic, asynchronous 'demand' signals. Almost all control-input signals and status-output signals are synchronized to these clocks, to simplify system design.

The input and output ports operate altogether independently of each other, unless the FIFO becomes either totally full or else totally empty. Data flow is initiated at a port by the rising edge of its corresponding clock, and is gated by the appropriate edge-sampled enable signals.

The following FIFO status flags monitor the extent to which the internal memory has been filled: Full, Almost-Full, Half-Full, Almost-Empty, and Empty. The Almost-Full and Almost-Empty flag offsets are programmable over the entire FIFO depth; but, during a reset operation, each of these is initialized to a default offset value of 63_{10} (LH540215) or 127_{10} (LH540225) FIFO-memory words, from the respective FIFO boundary. If this default offset value is satisfactory, no further programming is required.

After a reset operation during which the ***$\overline{EMODE}$*** control input was not asserted (was HIGH), these FIFOs operate in the IDT-Compatible Operating Mode. In this mode, each part is pin-compatible and functionally-compatible with the IDT72215B/25B part of similar depth and speed grade; and the ***Control Register*** is not even accessible or visible to the external-system logic which is controlling the FIFO, although it still performs the same control functions.

However, assertion of the $\overline{EMODE}$ control input during a reset operation leaves Control Register bits 00-05 set, and causes the FIFO to operate in the Enhanced Operating Mode. In essence, asserting $\overline{EMODE}$ chooses a different default state for the Control Register. The system optionally then may program the Control Register in any desired manner to activate or deactivate any or all of the Enhanced-Operating-Mode features which it can control, including selectable-clock-edge flag synchronization, and read inhibition when the data outputs are disabled.

Whenever $\overline{EMODE}$ is being asserted, interlocked-operation paralleling also is available, by appropriate interconnection of the FIFO's expansion inputs.

The retransmit facility is available during standalone operation, in either IDT-Compatible Operating Mode or Enhanced Operating Mode. (See Tables 1 and 2.) It is inoperative if the $\overline{FL}$/*RT* input signal is grounded. It is not an IDT72215B/25B feature. ***The Retransmit control signal causes the internal FIFO read-address pointer to be set back to zero, without affecting the internal FIFO write-address pointer. Thus, the Retransmit control signal also provides a mechanism whereby a block of data delimited by the zero physical address and the current write-address-pointer address may be read out repeatedly, an arbitrary number of times.***

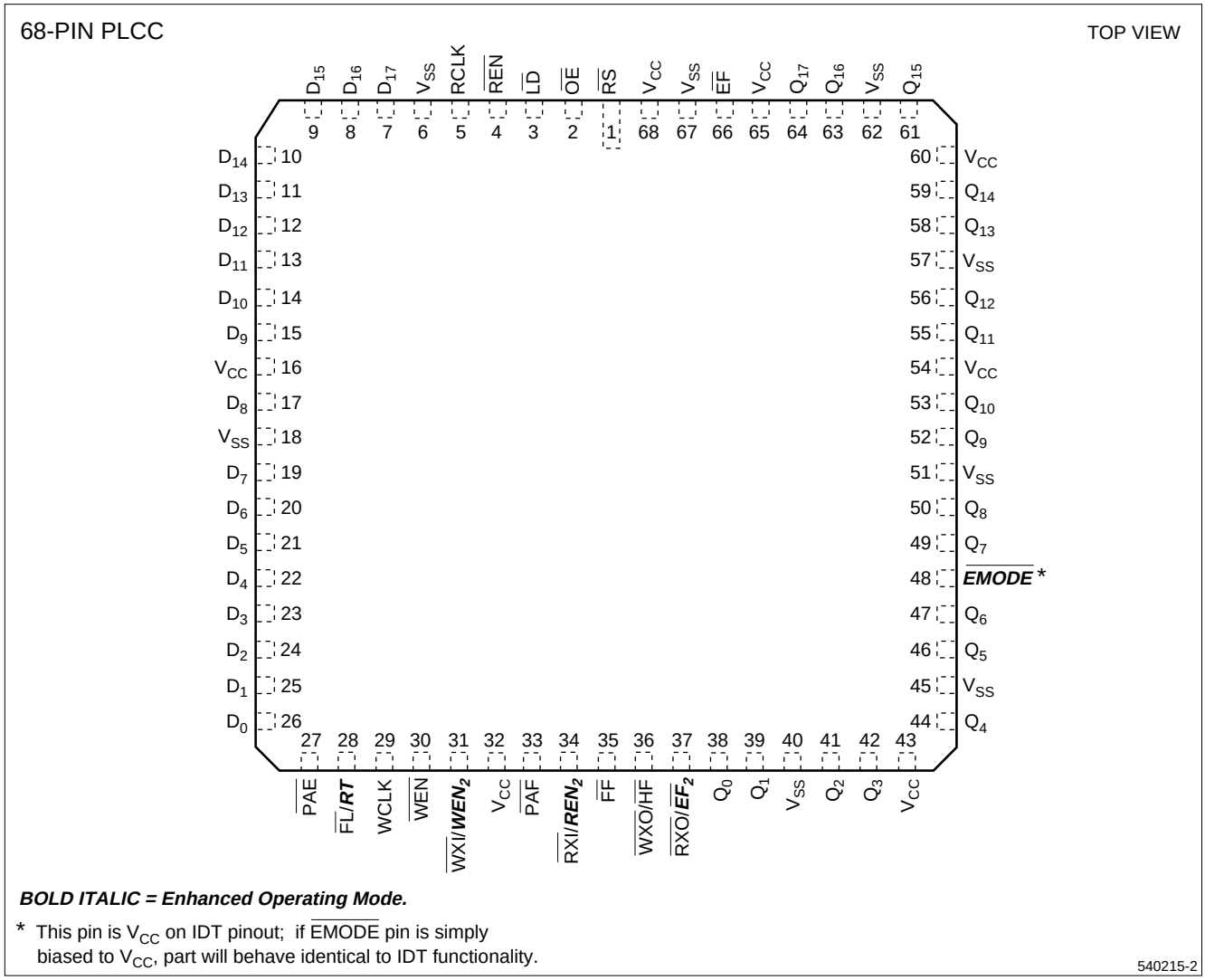
The only restrictions are that neither the read-address pointer nor the write-address pointer may 'wrap around' during this entire process, and that the retransmit facility is not available during depth-cascaded operation, either in IDT-Compatible Operating Mode or in Enhanced Operating Mode. (See Tables 1 and 2.) Also, the flags behave differently for a short time after a retransmit operation. Otherwise, the retransmit facility is available during standalone operation, in either IDT-Compatible Operating Mode or Enhanced Operating Mode.

Note that, when $\overline{FL}$/RT is being used as RT, RT is an assertive-HIGH signal, rather than assertive-LOW as it is in most other FIFOs having a retransmit facility.

Programming the programmable-flag offsets, ***the timing synchronization of the various status flags, the optional read-suppression functionality of $\overline{OE}$, and the behavior of the pointers which access the offset-value registers and the Control Register*** may be individually controlled by asserting the signal $\overline{LD}$, without any reset operation. When $\overline{LD}$ is being asserted, and writing is being enabled by asserting $\overline{WEN}$, some portion of the input bus word $D_0 – D_{17}$ is used at the next rising edge of WCLK to program one or more of the programmable registers on successive write clocks. Likewise, the values programmed into these programmable registers may be read out for verification by asserting $\overline{LD}$ and $\overline{REN}$, with the outputs $Q_0 – Q_{17}$ enabled. Reading out these programmable registers should not be initiated while they are being written into. Table 3 defines the possible modes of operation for loading and reading out the contents of programmable registers.

BOLD ITALIC = Enhanced Operating Mode

In the Enhanced Operating Mode, coordinated operation of two 18-bit FIFOs as one 36-bit FIFO may be ensured by 'interlocked' crosscoupling of the status-flag outputs from each FIFO to the expansion inputs of the other one; that is, $\overline{FF}$ to $\overline{WXI}/WEN_2$, and $\overline{EF}$ to $\overline{RXI}/REN_2$, in both directions between two paralleled FIFOs. This 'interlocked' operation takes effect automatically, if two paralleled FIFOs are crossconnected in this manner, with the $\overline{EMODE}$ control input being asserted (LOW). (See Tables 1 and 2, also Figures 27 and 30.) IDT-compatible depth cascading no longer is available when operating in this 'interlocked-paralleled' mode; however, pipelined depth cascading remains available.

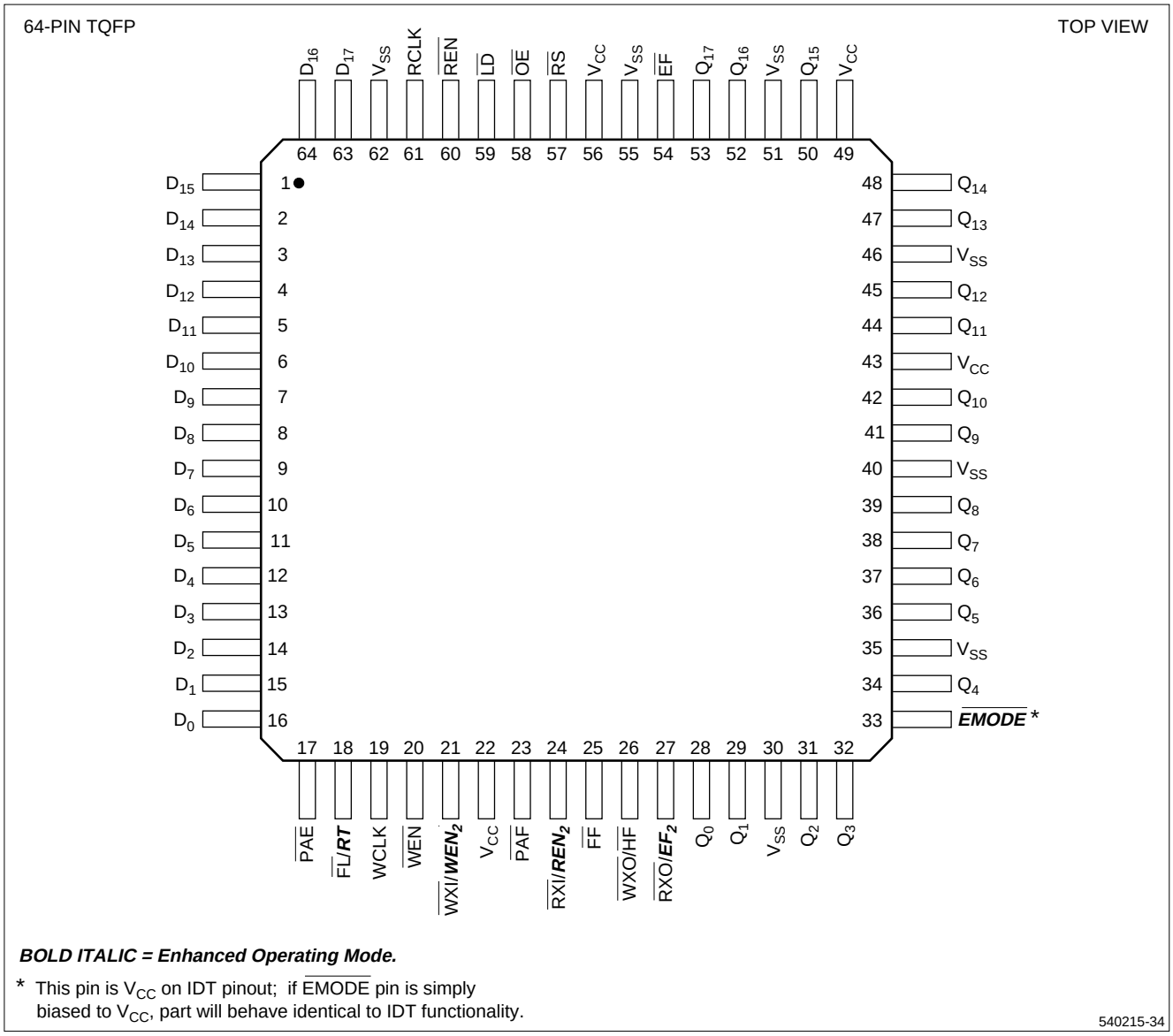


BOLD ITALIC = Enhanced Operating Mode.

* This pin is V_{CC} on IDT pinout; if $\overline{EMODE}$ pin is simply biased to V_{CC}, part will behave identical to IDT functionality.

540215-2

Figure 2. Pin Connections for 68-Pin PLCC Package



BOLD ITALIC = Enhanced Operating Mode.

* This pin is V_{CC} on IDT pinout; if $\overline{\text{EMODE}}$ pin is simply biased to V_{CC}, part will behave identical to IDT functionality.

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Figure 3. Pin Connections for 64-Pin TQFP Package

SUMMARY OF SIGNALS/PINS

PIN	NAME
$D_0 - D_{17}$	Data Inputs
$\overline{RS}$	Reset
$\overline{\textbf{\textit{EMODE}}}$	***Enhanced Operating Mode***
WCLK	Write Clock
$\overline{WEN}$	Write Enable
RCLK	Read Clock
$\overline{REN}$	Read Enable
$\overline{OE}$	Output Enable
$\overline{LD}$	Load
$\overline{FL}$***/RT***	First Load/***Retransmit***
$\overline{RXI}$***/REN2***	Read Expansion Input/***Read Enable 2***

PIN	NAME
$\overline{WXI}$***/WEN2***	Write Expansion Input/***Write Enable 2***
$\overline{FF}$	Full Flag
$\overline{PAF}$	Programmable Almost-Full Flag
$\overline{WXO}/\overline{HF}$	Write Expansion Output/Half-Full Flag
$\overline{PAE}$	Programmable Almost-Empty Flag
$\overline{EF}$	Empty Flag
$\overline{RXO}/\overline{\textbf{\textit{EF2}}}$	Read Expansion Output/***Empty Flag 2***
$Q_0 - Q_{17}$	Data Outputs
V_{CC}	Power
V_{SS}	Ground

BOLD ITALIC = Enhanced Operating Mode

PIN LIST

SIGNAL NAME	PLCC PIN NO.	TQFP PIN NO.
$\overline{RS}$	1	57
$\overline{OE}$	2	58
$\overline{LD}$	3	59
$\overline{REN}$	4	60
RCLK	5	61
D_{17}	7	63
D_{16}	8	64
D_{15}	9	1
D_{14}	10	2
D_{13}	11	3
D_{12}	12	4
D_{11}	13	5
D_{10}	14	6
D_9	15	7
D_8	17	8
D_7	19	9
D_6	20	10
D_5	21	11
D_4	22	12
D_3	23	13
D_2	24	14
D_1	25	15
D_0	26	16
$\overline{PAE}$	27	17
$\overline{FT}$/***RT***	28	18
WCLK	29	19
$\overline{WEN}$	30	20
$\overline{WXI}$/***WEN2***	31	21
$\overline{PAF}$	33	23
$\overline{RXI}$/***REN2***	34	24
$\overline{FF}$	35	25
$\overline{WXO}/\overline{HF}$	36	26
$\overline{RXO}/\overline{***EF2***}$	37	27
Q_0	38	28

SIGNAL NAME	PLCC PIN NO.	TQFP PIN NO.
Q_1	39	29
Q_2	41	31
Q_3	42	32
Q_4	44	34
Q_5	46	36
Q_6	47	37
$\overline{***EMODE***}$	48	33
Q_7	49	38
Q_8	50	39
Q_9	52	41
Q_{10}	53	42
Q_{11}	55	44
Q_{12}	56	45
Q_{13}	58	47
Q_{14}	59	48
Q_{15}	61	50
Q_{16}	63	52
Q_{17}	64	53
$\overline{EF}$	66	54
V_{SS}	6	62
V_{CC}	16	NC
V_{SS}	18	NC
V_{CC}	32	22
V_{SS}	40	30
V_{CC}	43	NC
V_{SS}	45	35
V_{SS}	51	40
V_{CC}	54	43
V_{SS}	57	46
V_{CC}	60	49
V_{SS}	62	51
V_{CC}	65	NC
V_{SS}	67	55
V_{CC}	68	56

BOLD ITALIC = Enhanced Operating Mode

PIN DESCRIPTIONS

PIN	NAME	PIN TYPE [1]	DESCRIPTION
$D_0 – D_{17}$	Data Inputs	I	Data inputs from an 18-bit bus.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is taken LOW, the FIFO's internal read and write pointers are set to address the first physical location of the RAM array; $\overline{FF}$, $\overline{PAF}$, and $\overline{HF}$ go HIGH; and $\overline{PAE}$ and $\overline{EF}$ go LOW. The programmable-flag-offset registers ***and the Control Register*** are set to their default values. (But see the description of ***EMODE***, below.) A reset operation is required before an initial read or write operation after power-up.
$\overline{EMODE}$	***Enhanced Operating Mode***	***I***	***When $\overline{EMODE}$ is tied LOW, the default setting for Control Register bits 00-05 after a reset operation changes to HIGH rather than LOW, thus enabling all Control-Register-controllable Enhanced Operating Mode features, and allowing access to the Control Register for reprogramming or readback. (See Tables 1, 2, and 5.) If this behavior is desired, EMODE may be grounded; however, Control Register bits 00-05 still may be individually programmed to selectively enable or disable certain of the Enhanced Mode features, even though those features associated with interlocked-paralleled operation always are enabled whenever EMODE is being asserted. (See Table 2.) Alternatively, EMODE may be tied to V_{CC}, so that the FIFO is functionally IDT-compatible, and the Control Register is not accessible or visible, and all of its bits remain LOW. Controlling EMODE dynamically during system operation is not recommended.***
WCLK	Write Clock	I	Data is written into the FIFO on a LOW-to-HIGH transition of WCLK, whenever $\overline{WEN}$ (Write Enable) is being asserted (LOW), and $\overline{LD}$ is HIGH. If $\overline{LD}$ is LOW, a programmable register rather than the internal FIFO memory is written into. ***In the Enhanced Operating Mode, WEN_2 is ANDed with $\overline{WEN}$ to produce an effective internal write-enable signal.*** [2]
$\overline{WEN}$	Write Enable	I	When $\overline{WEN}$ is LOW and $\overline{LD}$ is HIGH, an 18-bit data word is written into the FIFO on every LOW-to-HIGH transition of WCLK. When $\overline{WEN}$ is HIGH, the FIFO internal memory continues to hold the previous data. (See Table 3.) Data will not be written into the FIFO if $\overline{FF}$ is LOW. ***In the Enhanced Operating Mode, WEN_2 is ANDed with $\overline{WEN}$ to produce an effective internal write-enable signal.*** [2]
RCLK	Read Clock	I	Data is read from the FIFO on a LOW-to-HIGH transition of RCLK whenever $\overline{REN}$ (Read Enable) is being asserted (LOW), and $\overline{LD}$ is HIGH. If $\overline{LD}$ is LOW, a programmable register rather than the internal FIFO memory is read from. ***In the Enhanced Operating Mode, REN_2 is ANDed with $\overline{REN}$ (and whenever Control Register bit 05 is HIGH, also with $\overline{OE}$) to produce an effective internal read-enable signal.*** [2]
$\overline{REN}$	Read Enable	I	When $\overline{REN}$ is LOW and $\overline{LD}$ is HIGH, an 18-bit data word is read from the FIFO on every LOW-to-HIGH transition of RCLK. When $\overline{REN}$ is HIGH, and/or also when $\overline{EF}$ is LOW, the FIFO's output register continues to hold the previous data word, whether or not $Q_0 – Q_{17}$ (the data outputs) are enabled. (See Table 3.) ***In the Enhanced Operating Mode, REN_2 is ANDed with $\overline{REN}$ (and whenever Control Register bit 05 is HIGH, also with $\overline{OE}$) to produce an effective internal read-enable signal.*** [2]
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the FIFO's data outputs drive the bus to which they are connected. If $\overline{OE}$ is HIGH, the FIFO's outputs are in high-Z (high-impedance) state. ***In the Enhanced Operating Mode, $\overline{OE}$ not only continues to control the outputs in this same manner, but also can function as an additional ANDing input to the combined effective read-enable signal, along with $\overline{REN}$ and REN_2, whenever Control Register bit 05 is HIGH. (See Table 5.)*** [2]

[1] I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

[2] The ostensible differences in signal assertiveness are reconciled before ANDing.

BOLD ITALIC = Enhanced Operating Mode

PIN DESCRIPTIONS (cont'd)

PIN	NAME	PIN TYPE [1]	DESCRIPTION
$\overline{LD}$	Load	I	When $\overline{LD}$ is LOW, the data word on $D_0 - D_{17}$ (the data inputs) is written into a programmable-flag-offset register, ***or into the Control Register (when in the Enhanced Operating Mode),*** on the LOW-to-HIGH transition of WCLK, whenever $\overline{WEN}$ is LOW. (See Table 3.) Also, when $\overline{LD}$ is LOW, a word is read to $Q_0 - Q_{17}$ (the data outputs) from the offset registers ***and/or the Control Register (when in the Enhanced Operating Mode)*** on the LOW-to-HIGH transition of RCLK, whenever $\overline{REN}$ is LOW. (See again Table 3, and particularly the Notes following this table.) When $\overline{LD}$ is HIGH, normal FIFO write and read operations are enabled.
$\overline{FL}$***/RT***	First Load/ ***Retransmit***	I	In the standalone or paralleled configuration, $\overline{FL}$***/RT*** should be LOW during a reset operation. (See Tables 1 and 2.) ***However, thereafter, in the standalone or paralleled configuration, if FL is taken HIGH, it functions instead as RT (Retransmit), and resets the FIFO's internal read pointer to the first physical location of the RAM array. Note that although Retransmit is an 'enhanced' feature, it is always available for a FIFO during standalone operation, whether the FIFO is in IDT-Compatible Operating Mode or in Enhanced Operating Mode; it is not regulated either by the Control Register or by the EMODE control input.*** In IDT-compatible cascaded configuration, $\overline{FL}$ has an entirely different function; it is grounded for the first FIFO device (the 'master' device or 'first-load' device), and is set to HIGH for all other FIFO devices in the daisy chain. Thus, the ***Retransmit*** feature is not available for FIFOs operating in an IDT-compatible cascaded configuration.
$\overline{WXI}$***/WEN2***	Write Expansion Input/***Write Enable 2***	I	This signal is dual-purpose; its functionality is determined during a reset operation, according to its own state, and also according to the states of the three other control inputs $\overline{RXI}$***/REN2***, $\overline{FL}$***/RT***, and $\overline{EMODE}$. (See Tables 1 and 2.) In the standalone or paralleled configuration, $\overline{WXI}$/***WEN2*** is grounded. In the cascaded configuration, $\overline{WXI}$/***WEN2*** is connected to WXO (Write Expansion Output) of the previous device, and functions as WXI. ***In the Enhanced Operating Mode, $\overline{WXI}$/WEN2 functions as a second write-enable signal, WEN2, which is ANDed with WEN to produce an effective internal write-enable signal.*** [2]
$\overline{RXI}$***/REN2***	Read Expansion Input/***Read Enable 2***	I	This signal is dual-purpose; its functionality is determined during a reset operation, according to its own state, and also according to the states of the three other control inputs $\overline{WXI}$***/WEN2***, $\overline{FL}$***/RT***, and $\overline{EMODE}$. (See Tables 1 and 2.) In the standalone or paralleled configuration, $\overline{RXI}$/***REN2*** is grounded. In the cascaded configuration, $\overline{RXI}$/***REN2*** is connected to $\overline{RXO}$ (Read Expansion Output) of the previous device, and functions as $\overline{RXI}$. ***In the Enhanced Operating Mode, $\overline{RXI}$/REN2 functions as a second read-enable signal, REN2, which is ANDed with $\overline{REN}$ – and perhaps also with $\overline{OE}$, if Control-Register bit 05 is HIGH – to produce an effective internal read-enable signal.*** [2]
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full; further advancement of its internal write-address pointer, and further data writes through its Data Inputs into its internal memory array, are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
$\overline{PAF}$	Programmable Almost-Full Flag	O	When $\overline{PAF}$ is LOW, the FIFO is 'almost full,' based on the almost-full-offset value programmed into the FIFO's Almost-Full Offset Register. The default value of this offset at reset is one-eighth of the total number of words in the FIFO-memory array, minus one, measured from 'full.' (See Table 4.) In the IDT-Compatible Operating Mode, PAF is asynchronous. ***In the Enhanced Operating Mode, PAF is synchronized to WCLK after a reset operation, according to the state of Control Register bit 04. (See Table 5.)***

NOTES:
1. I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level
2. The ostensible differences in signal assertiveness are reconciled before ANDing.

BOLD ITALIC = Enhanced Operating Mode

PIN DESCRIPTIONS (cont'd)

PIN	NAME	PIN TYPE [1]	DESCRIPTION
$\overline{WXO}/\overline{HF}$	Write Expansion Output/ Half-Full Flag	O	This signal is dual-purpose; its functionality is determined during a reset operation according to the states of the two control inputs WXI/***WEN2*** and RXI/***REN2***. (See Tables 1 and 2.) In the standalone or paralleled configuration, whenever $\overline{HF}$ is LOW the device is more than half full. In IDT-Compatible Operating Mode, $\overline{HF}$ is asynchronous; ***in the Enhanced Operating Mode, HF may be synchronized either to WCLK or to RCLK after a reset operation, according to the state of Control Register bits 02 and 03. (See Table 5.)*** In the IDT-compatible cascaded configuration, a pulse is sent from WXO to the WXI input of the next FIFO in the daisy-chain cascade, whenever the last location in the FIFO is written.
$\overline{PAE}$	Programmable Almost-Empty Flag	O	When $\overline{PAE}$ is LOW, the FIFO is 'almost empty,' based on the almost-empty-offset value programmed into the FIFO's Almost-Empty Offset Register. The default value of this offset at reset is one-eighth of the total number of words in the FIFO-memory array, minus one, measured from 'empty.' (See Table 4.) In IDT-Compatible Operating Mode, $\overline{PAE}$ is asynchronous. ***In the Enhanced Operating Mode, $\overline{PAE}$ is synchronized to RCLK after a reset operation, according to the state of Control Register bit 01. (See Table 5.)***
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty; further advancement of its internal read-address pointer, and further readout of data words from its internal memory array to its Data Outputs, are inhibited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{RXO}$/***$\overline{EF_2}$***	Read Expansion Output	O	This signal is dual-purpose; its functionality is determined by the state of the ***EMODE*** control input during a reset operation. (See Tables 1 and 2.) In the IDT-Compatible Operating Mode, in a cascaded configuration, a pulse is sent from $\overline{RXO}$ to the $\overline{RXI}$ input of the next FIFO in the daisy-chain cascade, whenever the last location of the FIFO is read. ***In the Enhanced Operating Mode, whenever $\overline{EMODE}$ is being asserted (LOW), $\overline{EF_2}$ behaves as an exact duplicate of $\overline{EF}$, but delayed by one full cycle of RCLK with respect to $\overline{EF}$.***
$Q_0 - Q_{17}$	Data Outputs	O/Z	Data outputs to drive an 18-bit bus.
V_{CC}	Power	V	+5 V power-supply pins.
V_{SS}	Ground	V	0 V ground pins.

NOTE:

1. I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

BOLD ITALIC = Enhanced Operating Mode

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	–0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential	–0.5 V to V_{CC} + 0.5 V
DC Output Current [1]	±75 mA
Temperature Range with Power Applied [2]	–55°C to 125°C
Storage Temperature Range	–65°C to 150°C
Power Dissipation (PLCC Package Limit)	2 W

NOTES:
1. Only one output may be shorted at a time, for a period not exceeding 30 seconds.
2. Measured with clocks idle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T_A	Temperature, Ambient	0	70	C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage	–0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.0	V_{CC} + 0.5	V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
I_{LI}	Input Leakage	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	–10	10	µA
I_{LO}	I/O Leakage	$\overline{OE} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	–10	10	µA
V_{OH}	Output HIGH Voltage	I_{OH} = –12.0 mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16.0 mA		0.4	V
I_{CC}	Average Operating Supply Current [1]	Measured at f_{CC} = 50 MHz		190	mA
I_{CC2}	Average Standby Supply Current	All inputs = V_{IH} MIN. (clocks idle)		25	mA
I_{CC3}	Power-Down Supply Current	All inputs = V_{CC} – 0.2 V (clocks idle)		1	mA

NOTE:
1. Output load is disconnected.

AC TEST CONDITIONS

PARAMETER		RATING
Input Pulse Levels		V_{SS} to 3 V
Input Rise and Fall Times (10% to 90%)		3 ns
Input Timing Reference Levels		1.5 V
Output Timing Reference Levels		1.5 V
Output Load, Timing Tests (Figure 4)	R_1 (Top Resistor)	1.1k Ω
	R_2 (Bottom Resistor)	680 Ω
	C_L (Load Capacitance)	30 pF

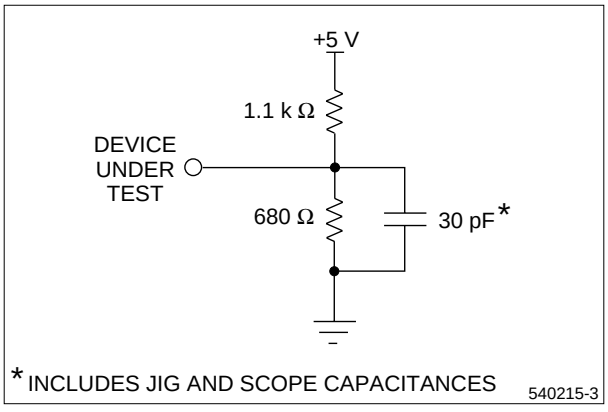


Figure 4. Output Load Circuit

CAPACITANCE[1, 2]

PARAMETER	RATING
C_{IN} (Input Capacitance) V_{IN} = 0 V	8 pF
C_{OUT} (Output Capacitance) V_{OUT} = 0 V	8 pF

NOTES:
1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0 MHz, with V_{IN} = 0 V.

BOLD ITALIC = Enhanced Operating Mode

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	–20		–25		-35	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
f_{CC}	Clock Cycle Frequency		50		40		28.6
t_A	Data Access Time	2	12	3	15	3	20
t_{CLK}	Clock Cycle Time	20		25		35	
t_{CLKH}	Clock HIGH Time	8		10		14	
t_{CLKL}	Clock LOW Time	8		10		14	
t_{DS}	Data Setup Time	5		6		7	
t_{DH}	Data Hold Time	2		2		2	
t_{ENS}	Enable Setup Time	5		6		7	
t_{ENH}	Enable Hold Time	2		2		2	
t_{RS}	Reset Pulse Width [1]	20		25		35	
t_{RSS}	Reset Setup Time [2]	12		15		20	
t_{RSR}	Reset Recovery Time [2]	12		15		20	
t_{RSF}	Reset to Flag and Output Time		30		35		40
t_{OLZ}	Output Enable to Output in Low-Z [2]	0		0		0	
t_{OE}	Output Enable to Output Valid		9		12		15
t_{OHZ}	Output Enable to Output in High-Z [2]	1	9	1	12	1	15
t_{WFF}	Write Clock to Full Flag		12		15		20
t_{REF}	Read Clock to Empty Flag		12		15		20
t_{PAF}	Clock to Programmable Almost-Full Flag (IDT-Compatible Operating Mode)		14		17		23
t_{PAE}	Clock to Programmable Almost-Empty Flag (IDT-Compatible Operating Mode)		14		17		23
t_{HF}	Clock to Half-Full Flag (IDT-Compatible Operating Mode)		14		17		23
t_{PAFS}	***Clock to Programmable Almost-Full Flag (Enhanced Operating Mode)***		***14***		***17***		***23***
t_{PAES}	***Clock to Programmable Almost-Empty Flag (Enhanced Operating Mode)***		***14***		***17***		***23***
t_{HFS}	***Clock to Half-Full Flag (Enhanced Operating Mode)***		***14***		***17***		***23***
t_{XO}	Clock to Expansion-Out		12		15		20
t_{XI}	Expansion-In Pulse Width	7		9		13	
t_{XIS}	Expansion-In Setup Time	7		9		14	
t_{SKEW1}	Skew Time Between Read Clock and Write Clock for Full Flag [3]	9		11		16	
t_{SKEW2}	Skew Time Between Write Clock and Read Clock for Empty Flag [4]	9		11		16	

NOTES:

1. Pulse widths less than the stated minimum values may cause incorrect operation.
2. Values are guaranteed by design; not currently tested.
3. These times also apply to the Programmable-Almost-Full and Half-Full flags when they are synchronized to WCLK.
4. These times also apply to the Half-Full and Programmable-Almost-Empty flags when they are synchronized to RCLK.

BOLD ITALIC = Enhanced Operating Mode

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES

Table 1. Grouping-Mode Determination During a Reset Operation [5]

$\overline{EMODE}$	$\overline{WXI}$/*WEN2*	$\overline{RXI}$/*REN2*	$\overline{FL}$/*RT*	MODE	$\overline{WXO}$/$\overline{HF}$ USAGE	$\overline{WXI}$/*WEN2* USAGE	$\overline{RXI}$/*REN2* USAGE	$\overline{FL}$/*RT* USAGE	$\overline{RXO}$/*EF2* USAGE
H [1]	H	H	H	Cascaded Slave [2]	$\overline{WXO}$	$\overline{WXI}$	$\overline{RXI}$	$\overline{FL}$	$\overline{RXO}$
H [1]	H	H	L	Cascaded Master [2]	$\overline{WXO}$	$\overline{WXI}$	$\overline{RXI}$	$\overline{FL}$	$\overline{RXO}$
H	H	L	X	(Reserved)	–	–	–	–	–
H	L	H	X	(Reserved)	–	–	–	–	–
H	L	L	H [3]	(Not Allowed During Reset)	($\overline{HF}$)	(none)	(none)	***(RT)***	(none)
H	L	L	L [3]	Standalone	$\overline{HF}$	(none)	(none)	***RT***	(none)
L	***X***	***X***	***H*** [3]	***(Not Allowed During Reset)***	***($\overline{HF}$)***	***(WEN2)***	***(REN2)***	***(RT)***	***($\overline{EF}$2)***
L	***X***	***X***	***L*** [3]	***Interlocked Paralleled*** [4]	***$\overline{HF}$***	***WEN2***	***REN2***	***RT***	***$\overline{EF}$2***

NOTES:

1. In IDT-compatible cascading, a reset operation forces $\overline{WXO}$/$\overline{HF}$ and $\overline{RXO}$/***$\overline{EF}$2*** HIGH for the nth FIFO, thus forcing $\overline{WXI}$/***WEN2*** and $\overline{RXI}$/***REN2*** HIGH for the (n + 1)st FIFO.
2. The terms 'master' and 'slave' refer to IDT-compatible cascading. In pipelined cascading[4], there is no such distinction.
3. ***Once grouping mode has been determined during a reset operation, $\overline{FL}$/RT then may go HIGH to activate a retransmit operation.***
4. ***$\overline{EMODE}$ must be asserted for access to the Control Register to be enabled. Also, FIFOs being used in a pipelined-cascading configuration should be in Interlocked Paralleled mode.***
5. Setup-time and recovery-time specifications apply during a reset operation.
6. H = HIGH; L = LOW; X = Don't Care.

Table 2. Expansion-Pin Usage According to Grouping Mode

I/O	PIN	IDT-COMPATIBLE OPERATING MODE			ENHANCED OPERATING MODE
		DEPTH-CASCADED MASTER	DEPTH-CASCADED SLAVE	STANDALONE	*INTERLOCKED PARALLELED*
I	$\overline{WXI}$ /***WEN2***	From $\overline{WXO}$ ((n-1)st FIFO)	From $\overline{WXO}$ ((n-1)st FIFO)	Grounded	***From $\overline{FF}$ (other FIFO)***
O	$\overline{WXO}$/$\overline{HF}$	To $\overline{WXI}$ ((n+1)st FIFO)	To $\overline{WXI}$ ((n+1)st FIFO)	Becomes $\overline{HF}$	***Becomes $\overline{HF}$***
I	$\overline{RXI}$/***REN2***	From $\overline{RXO}$ ((n-1)st FIFO)	From $\overline{RXO}$ ((n-1)st FIFO)	Grounded	***From $\overline{EF}$ (other FIFO)***
O	$\overline{RXO}$***/$\overline{EF}$2***	To $\overline{RXI}$ ((n+1)st FIFO)	To $\overline{RXI}$ ((n+1)st FIFO)	Unused	***Becomes $\overline{EF}$2***
I	$\overline{FL}$/***RT***	Grounded (Logic LOW)	Logic HIGH	***Becomes RT*** [1]	***Becomes RT*** [1]

NOTE:

1. $\overline{FL}$/***RT*** may be grounded if ***the Retransmit facility*** is not being used.

BOLD ITALIC = Enhanced Operating Mode

Table 3. Selection of Read and Write Operations

$\overline{LD}$	$\overline{WEN}$ [3,4]	$\overline{REN}$ [3, 4]	WCLK	RCLK	ACTION
L	X	X	–	–	No operation.
L	L	L	∧	∧	Illegal combination, which will cause errors.
L	L	H	∧	X	Write to a programmable register. [1]
L	H	H	∧	X	Hold present value of programmable-register write counter, and do not write. [2]
L	H	L	X	∧	Read from a programmable register. [1]
L	H	H	X	∧	Hold present value of programmable-register read counter, and do not read. [2]
H	L	X	∧	X	Normal FIFO write operation.
H	X	L	X	∧	Normal FIFO read operation.
H	L	X	–	X	No write operation.
H	H	X	X	X	No write operation.
H	X	L	X	–	No read operation.
H	X	H	X	X	No read operation.
H	L	L	–	–	No operation.

KEY:

H = Logic 'HIGH'; L = Logic 'LOW'; X = 'Don't-care' (logic 'HIGH,' logic 'LOW,' or any transition);

∧ = A 'LOW'-to-'HIGH' transition; – = Any condition EXCEPT a 'LOW'-to-'HIGH' transition.

NOTES:

1. The selection of a programmable register to be written or read is controlled by two simple state machines. One state machine controls the selection for writing; the other state machine controls the selection for reading. These two state machines operate independently of each other. Both state machines are reset to point to Word 0 by a reset operation. ***In the Enhanced Operating Mode, if Control Register bit 00 is set, both state machines are also reset to point to Word 0 by deassertion of LD after LD has been asserted (that is, by a rising edge of LD), followed by a valid memory array write cycle for the writing-control state machine and/or by a valid memory array read cycle for the reading-control state machine.***
2. The order of the two programmable registers which are accessible in IDT-Compatible Operating Mode, as selected by either state machine, is always:
   Word 0: Almost-Empty Offset Register
   Word 1: Almost-Full Offset Register
   Word 0: Almost-Empty Offset Register
   ...
   (repeats indefinitely)
   ...

   The order of the three programmable registers which are accessible in Enhanced Operating Mode, as selected by either state machine, is always:
   Word 0: Almost-Empty Offset Register
   Word 1: Almost-Full Offset Register
   Word 2: Control Register
   Word 0: Almost-Empty Offset Register
   ...
   (repeats indefinitely)

   Note that, in IDT-Compatible Operating Mode, Word 2 is not accessed; Word 0 and Word 1 alternate.
3. After normal FIFO operation has begun, writing new contents into either of the offset registers should only be done when the FIFO is empty.
4. ***WEN_2, REN_2, and $\overline{OE}$ may be ANDed terms in the enabling of read and write operations, according to the state of the $\overline{EMODE}$ control input and of Control Register Bit 05.***

BOLD ITALIC = Enhanced Operating Mode

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES (cont'd)

Table 4. Status Flags

NUMBER OF UNREAD DATA WORDS PRESENT WITHIN FIFO [1, 2]		FULL FLAG	MIDDLE FLAGS			EMPTY FLAG
512 × 18 FIFO	**1024 × 18 FIFO**	$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
0	0	H	H	H	L	L
1 to q	1 to q	H	H	H	L	H
(q + 1) to 256	(q + 1) to 512	H	H	H	H	H
257 to (512 – (p + 1))	513 to (1024 – (p + 1))	H	H	L	H	H
(512 – p) to 511	(1024 – p) to 1023	H	L	L	H	H
512	1024	L	L	L	H	H

NOTES:

1. q = Programmable-Almost-Empty Offset value. (Default values: 512 × 18, q = 63; 1024 × 18, q = 127.)
2. p = Programmable-Almost-Full Offset value. (Default values: 512 × 18, p = 63; 1024 × 18, p = 127.)
3. Only 9 (512 × 18) or 10 (1024 × 18) of the 12 offset-value-register bits should be programmed. The unneeded most-significant-end bits should be LOW (zero).
4. The flag output is delayed by one full clock cycle in Enhanced Operating Mode, when synchronous operation is specified for intermediate flags.

BOLD ITALIC = Enhanced Operating Mode

Table 5. Control-Register Format

COMMAND REGISTER BITS	CODE	VALUE AFTER RESET		FLAG AFFECTED, IF ANY	DESCRIPTION	NOTES
		$\overline{EMODE}$ = H	$\overline{EMODE}$ = L			
00	L	L	H	–	Deassertion of $\overline{LD}$ does not reset the programmable-register write pointer and read pointer.	IDT-compatible addressing of programmable registers.
	H				Deassertion of $\overline{LD}$ resets the programmable-register write pointer and read pointer to address Word 0, the Programmable-Almost-Empty-Flag-Offset Register. The change takes effect after a valid write operation or a valid read operation, respectively, to the memory array.	Non-ambiguous addressing of programmable registers.
01	L	L	H	$\overline{PAE}$	Set by ↑RCLK, reset by ↑WCLK.	Asynchronous flag clocking.
	H				Set and reset by ↑RCLK.	Synchronous flag clocking.
03, 02	LL	LL	HH	$\overline{HF}$	Set by ↑WCLK, reset by ↑RCLK.	Asynchronous flag clocking.
	LH				Set and reset by ↑RCLK.	Synchronous flag clocking at output port.
	HL, HH				Set and reset by ↑WCLK.	Synchronous flag clocking at input port.
04	L	L	H	$\overline{PAF}$	Set by ↑WCLK, reset by ↑RCLK.	Asynchronous flag clocking.
	H				Set and reset by ↑WCLK.	Synchronous flag clocking.
05	L	L	H	–	$\overline{OE}$ has no effect on an internal read operation, apart from disabling the outputs.	Allows the read-address pointer to advance even when $Q_0 – Q_{17}$ are not driving the output bus.
	H				Deassertion of $\overline{OE}$ inhibits a read operation; whenever the data outputs $Q_0 – Q_{17}$ are in the high-Z state, the read pointer does not advance.	Inhibits the read-address pointer from advancing when $Q_0 – Q_{17}$ are not driving the output bus; thus, guards against data loss.
06	L	L	L	–	Reserved.	Future use to control depth cascading and interlocked paralleling.
	H					
11, 10, 09, 08, 07	LLLLL	LLLLL	LLLLL	–	Reserved.	Reserved.

NOTES:

1. When $\overline{EMODE}$ is HIGH, and ***Control Register bits 00-05 are LOW,*** the FIFO behaves in a manner functionally equivalent to the IDT72215B/25B FIFO of similar depth and speed grade. Under these conditions, the ***Control Register*** is not visible or accessible to the external system which includes the FIFO.
2. If $\overline{EMODE}$ is not asserted (is HIGH), ***Control Register bits 00-05 remain LOW*** after a reset operation. ***However, if $\overline{EMODE}$ is asserted (is LOW) during a reset operation, Control Register bits 00-05 are forced HIGH, and remain HIGH until changed. Control Register bits 06-11 are unaffected by EMODE.***

BOLD ITALIC = Enhanced Operating Mode

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES (cont'd)

Data Inputs

DATA IN ($D_0 – D_{17}$)

Data, programmable-flag-offset values, and ***Control-Register*** codes are input to the FIFO as 18-bit words on $D_0 – D_{17}$. Unused bit positions in offset-value ***and Control-Register*** words should be zero-filled.

Control Inputs

RESET ($\overline{RS}$)

The FIFO is reset whenever the asynchronous Reset ($\overline{RS}$) input is taken to a LOW state. A reset operation is required after power-up, before the first write operation may occur. The state of the FIFO is fully defined after a reset operation. If the default values which are entered into the Programmable-Flag-Offset-Value Registers ***and the Control Register*** by a reset operation are acceptable, then no device programming is required. A reset operation initializes the FIFO's internal read-address and write-address pointers to the FIFO's first physical memory location. The five status flags, $\overline{FF}$, $\overline{PAF}$, $\overline{HF}$, $\overline{PAE}$, and $\overline{EF}$, are updated to indicate that the FIFO is completely empty; thus, the first three of these are reset to HIGH, and the last two are reset to LOW. The flag-offset values for $\overline{PAF}$ and $\overline{PAE}$ each are initialized to one-eighth of the depth of a single FIFO, minus one; 63 for a 512-word FIFO, and 127 for a 1024-word FIFO. If ***$\overline{EMODE}$*** is not being asserted (i.e., if ***$\overline{EMODE}$*** is HIGH), all ***Control Register*** bits are initialized to LOW, to configure the FIFO to operate in the IDT72215B/25B-Compatible Operating Mode. Until a write operation occurs, the data outputs $D_0 – D_{17}$ all are LOW whenever $\overline{OE}$ is LOW.

ENHANCED OPERATING MODE ($\overline{EMODE}$)

Whenever $\overline{EMODE}$ is asserted during a reset operation, Control Register bits 00 – 05 remain HIGH rather than LOW after the completion of the reset operation. Thus, $\overline{EMODE}$ has the effect of activating all of the Enhanced-Operating-Mode features during a reset operation. Subsequently, they may be individually disabled or re-enabled by changing the setting of Control-Register bits. The behavior of these Enhanced-Operating-Mode features is described in Table 5. For permanent Enhanced-Operating-Mode operation, $\overline{EMODE}$ must be grounded; dynamic control of $\overline{EMODE}$ during system operation is not recommended.

Asserting $\overline{EMODE}$ during a reset operation also causes $\overline{WXI}/WEN_2$ to be configured as WEN_2, and $\overline{RXI}/REN_2$ to be configured as REN_2, to support interlocked-paralleled operation of two FIFOs 'side by side. (See Figure 27.) Additionally, $\overline{RXO}/\overline{EF}_2$ is configured as $\overline{EF}_2$, which duplicates the $\overline{EF}$ signal with one extra RCK cycle delay, in order to provide proper timing for 'pipelined' cascaded operation.

WRITE CLOCK (WCLK)

A rising edge (LOW-to-HIGH transition) of WCLK initiates a FIFO write cycle if $\overline{LD}$ is HIGH, or a programmable-register write cycle if $\overline{LD}$ is LOW. The 18 data inputs, and all input-side synchronous control inputs, must meet setup and hold times with respect to the rising edge of WCLK. The input-side status flags are meaningful after specified time intervals, following a rising edge of WCLK.

Conceptually, the WCLK input receives a free-running, periodic 'clock' waveform, which is used to control other signals which are edge-sensitive. However, there actually is not any absolute requirement that the WCLK waveform *must* be periodic. An 'asynchronous' mode of operation is in fact possible, if $\overline{WEN}$ is continuously asserted (that is, is continuously held LOW), and WCLK receives aperiodic 'clock' pulses of suitable duration. There likewise is no requirement that WCLK must have any particular synchronization relation to the read clock RCLK. These two clock inputs may in fact receive the same 'clock' signal; or they may receive totally-different signals, which are not synchronized to each other in any way.

WRITE ENABLE ($\overline{WEN}$)

Whenever $\overline{WEN}$ is being asserted (is LOW) and $\overline{LD}$ is HIGH, and the FIFO is not full, an 18-bit data word is loaded into the effective input register for the memory array at every WCLK rising edge (LOW-to-HIGH transition). Data words are stored into the two-port memory array sequentially, regardless of any ongoing read operation. Whenever $\overline{WEN}$ is not being asserted (is HIGH), the input register retains whatever data word it contained previously, and no new data word gets loaded into the memory array.

To prevent overrunning the internal FIFO boundaries, further write operations are inhibited whenever the Full Flag ($\overline{FF}$) is being asserted (is LOW). If a valid read operation then occurs, upon the completion of that read cycle $\overline{FF}$ again goes HIGH after a time t_{WFF}, and another write operation is allowed to begin whenever WCLK makes another LOW-to-HIGH transition. Effectively, $\overline{WEN}$ is overridden by $\overline{FF}$; thus, during normal FIFO operation, $\overline{WEN}$ has no effect when the FIFO is full.

In the Enhanced Operating Mode, whenever $\overline{EMODE}$ is being asserted (is LOW), $\overline{WXI}/WEN_2$ functions as WEN_2, an additional duplicate (albeit assertive-HIGH) write-enable input, in order to provide an'interlocking' mechanism for reliable synchronization of two paralleled FIFOs. To control writing, WEN_2 is ANDed with $\overline{WEN}$; this logic-AND function ($\overline{WEN} \bullet WEN_2$) then behaves like $\overline{WEN}$ in the foregoing description.

BOLD ITALIC = Enhanced Operating Mode

READ CLOCK (RCLK)

A rising edge (LOW-to-HIGH transition) of RCLK initiates a FIFO read cycle if $\overline{LD}$ is HIGH, or a programmable-register read cycle if $\overline{LD}$ is LOW. All output-side synchronous control inputs must meet setup and hold times with respect to the rising edge of RCLK. The 18 data outputs, and the output-side status flags, are meaningful after specified time intervals, following a rising edge of RCLK.

Conceptually, the RCLK input receives a free-running, periodic 'clock' waveform, which is used to control other signals which are edge-sensitive. However, there actually is not any absolute requirement that the RCLK waveform *must* be periodic. An 'asynchronous' mode of operation is in fact possible, if $\overline{REN}$ is continuously asserted (that is, is continuously held LOW), and RCLK receives aperiodic 'clock' pulses of suitable duration. There likewise is no requirement that RCLK must have any particular synchronization relation to the write clock WCLK. These two clock inputs may in fact receive the same 'clock' signal; or they may receive totally-different signals, which are not synchronized to each other in any way.

READ ENABLE ($\overline{REN}$)

Whenever $\overline{REN}$ is being asserted (is LOW), and the FIFO is not empty, an 18-bit data word is loaded into the output register from the memory array at every RCLK rising edge (LOW-to-HIGH transition). Data words are read from the two-port memory array sequentially, regardless of any ongoing write operation. Whenever $\overline{REN}$ is not being asserted (is HIGH), the output register retains whatever data word it contained previously, and no new data word gets loaded into it from the memory array.

To prevent underrunning the internal FIFO boundaries, further read operations are inhibited whenever the Empty Flag ($\overline{EF}$) is being asserted (is LOW). If a valid write operation then occurs, upon the completion of that write cycle $\overline{EF}$ again goes HIGH after a time t_{REF}, and another read operation is allowed to begin whenever RCLK makes another LOW-to-HIGH transition. Effectively, $\overline{REN}$ is overridden by $\overline{EF}$; thus, during normal FIFO operation, $\overline{REN}$ has no effect when the FIFO is empty.

In the Enhanced Operating Mode, one (or, sometimes two) additional read-enable inputs may be ANDed with $\overline{REN}$ to control reading, depending on the state of Control-Register Bit 05. The additional read-enable input(s) are REN_2 (and $\overline{OE}$).

Whenever $\overline{EMODE}$ is being asserted (is LOW), $\overline{RXI}/REN_2$ functions as REN_2, an additional duplicate (albeit assertive-HIGH) Read-Enable input, in order to provide an 'interlocking' mechanism for reliable synchronization of two paralleled FIFOs.

Also, if Control Register bit 05 has been set, $\overline{OE}$ takes on the extra role of serving as yet another duplicate read-enable input, in addition to its usual function of controlling the FIFO's data outputs, in order to inhibit further read operations whenever the FIFO's data outputs are disabled, and thereby to prevent data loss under some circumstances.

OUTPUT ENABLE ($\overline{OE}$)

$\overline{OE}$ is an assertive-LOW, asynchronous, output enable. In the IDT-Compatible Operating Mode, $\overline{OE}$ has only the effect of enabling or disabling the data outputs $Q_0 - Q_{17}$. That is, disabling $Q_0 - Q_{17}$ does not inhibit a read operation, for data being transmitted to the output register; the same data will remain available later, when the outputs are again enabled, unless subsequently overwritten. When $Q_0 - Q_{17}$ are enabled, each of these 18 data outputs is in a normal HIGH or LOW state, according to the bit pattern of the data word in the output register. When $Q_0 - Q_{17}$ are disabled, each of these outputs is in the high-Z (high-impedance) state.

In the Enhanced Operating Mode, if Control Register bit 05 has been set, $\overline{OE}$ behaves as an additional read-enable control input, as well as enabling and disabling the data outputs $Q_0 - Q_{17}$. Under these circumstances, incrementing the read-address pointer is inhibited whenever $Q_0 - Q_{17}$ are in the high-Z state. Thus, 'reading' successive words which fail ever to reach the outputs is prevented, as a safeguard against data loss.

LOAD ($\overline{LD}$)

The Sharp LH540215/25 FIFOs contain ***three*** 18-bit programmable registers. The contents of these three registers may be loaded with data from the data inputs $D_0 - D_{17}$, or read out onto the data outputs $Q_0 - Q_{17}$. The first two registers are the Programmable-Flag-Offset-Value Registers, for the Programmable Almost-Empty Flag ($\overline{PAE}$) and the Programmable Almost-Full Flag ($\overline{PAF}$) respectively. ***The third register is the Control Register, which includes several configuration-control bits for selectively enabling and disabling Sharp's Enhanced-Operating-Mode features.***

None of these three registers makes use of all of its available 18 bits. Figure 5 shows which bit positions of each register are operational. The two Programmable-Flag-Offset-Value Registers each contain an offset value in bits 0-8 (LH540215) or bits 0 – 9 (LH540225); bits 9 – 17 (LH540215) or bits 10 – 17 (LH540225) are unused. The default values for both offsets are one-eighth of the total number of words in the FIFO memory array, minus one: 63 for a 512 × 18 FIFO, and 127 for a 1024 × 18 FIFO.

BOLD ITALIC = Enhanced Operating Mode

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES (cont'd)

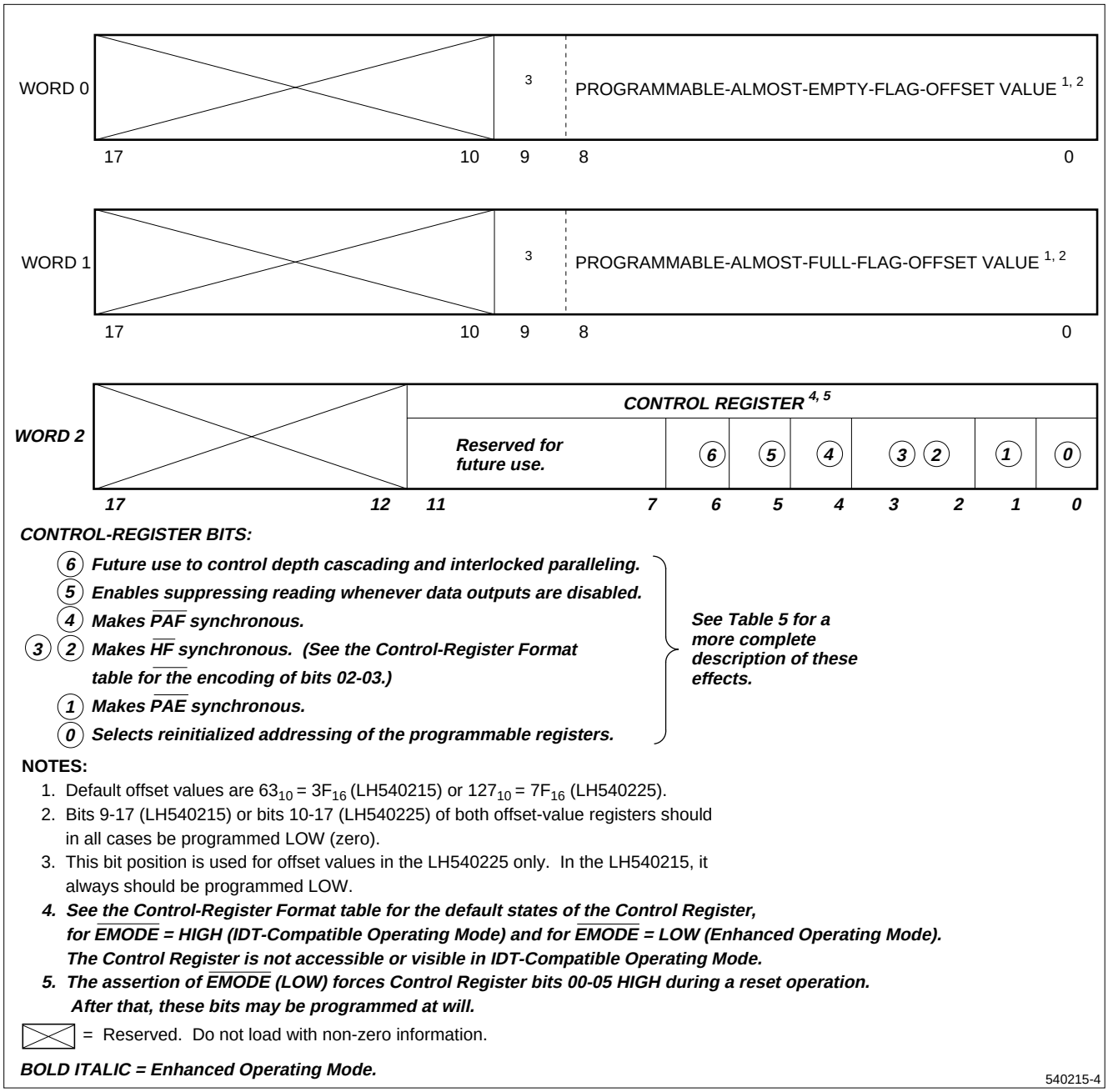


Figure 5. Programmable Registers

The ***Control Register*** configuration is shown in Figure 5 and in Table 5. For the ***Control Register***, in the IDT-Compatible Operating Mode, with ***$\overline{EMODE}$*** deasserted (HIGH), the default value for all Control-Register bits is zero (LOW). ***In the Enhanced Operating Mode, with $\overline{EMODE}$ asserted (LOW), the default value for bits 00-05 is HIGH, and the default value for bits 06-11 is LOW.***

Whenever $\overline{LD}$ and $\overline{WEN}$ are simultaneously being asserted (are both LOW), the 18-bit data word from the data inputs $D_0 - D_{17}$ is written into the Programmable-Almost-Empty-Flag-Offset-Value Register at the first rising edge (LOW-to-HIGH transition) of the write clock (WCLK). (See Table 3.) If $\overline{LD}$ and $\overline{WEN}$ continue to be simultaneously asserted, another 18-bit data word from the data inputs $D_0 - D_{17}$ is written into the Programmable-Almost-Full-Flag-Offset-Value Register at the second rising edge of WCLK.

What happens next is determined by the state of the ***$\overline{EMODE}$*** control input. If it is deasserted (HIGH), the next 18-bit word from the data inputs $D_0 - D_{17}$ is written back into the Programmable-Almost-Empty-Flag-Offset-Value Register again.

BOLD ITALIC = Enhanced Operating Mode

But, if $\overline{EMODE}$ is asserted (LOW), then still another 18-bit data word from the data inputs $D_0 – D_{17}$ is written into the Control Register at the third rising edge of WCLK. At the fourth rising edge of WCLK, writing again occurs to the Programmable-Almost-Empty-Flag-Offset-Value Register; and the same three-step writing sequence gets repeated on subsequent WCLK rising edges.

The lower nine bits of these offset-value words are made use of by the 512-word LH540215, and the lower ten bits by the 1024-word LH540225. ***Six active bits are used for the Control Register, by both the LH540215 and the LH540225.*** There is no restriction on the values which may occur in these offset-value ***and Control-Register*** fields. However, ***reserved*** bit positions must be encoded LOW, in order to maintain forward compatibility.

Writing contents to these two ***or three*** programmable registers does not have to occur all at one time, or to be effected by one single sequence of steps. Whenever $\overline{LD}$ is being asserted (is LOW) but $\overline{WEN}$ is not being asserted (is HIGH), the FIFO's internal programmable-register-write-address pointer maintains its present value, without any writing actually taking place at each rising edge of WCLK. (See Table 3.) Thus, for instance, one or two programmable registers may be written, after which the FIFO may be returned to normal FIFO-array-read/write operation by deasserting $\overline{LD}$ (to HIGH).

Likewise, whenever $\overline{LD}$ and $\overline{REN}$ are simultaneously being asserted (are both LOW) the 18-bit data word (zero-filled as necessary) from the Programmable-Almost-Empty-Flag-Offset-Value Register is read to the data outputs $Q_0 – Q_{17}$ at the first rising edge (LOW-to-HIGH transition) of the read clock (RCLK). (See Table 3.) If $\overline{LD}$ and $\overline{REN}$ continue to be simultaneously asserted, another 18-bit data word from the Programmable-Almost-Full-Flag-Offset-Value Register is read to the data outputs $Q_0 – Q_{17}$ at the second rising edge of RCLK.

What happens next is determined by the state of the ***$\overline{EMODE}$*** control input. If it is deasserted (HIGH), the next 18-bit word again comes from the Programmable-Almost-Empty-Flag-Offset-Value Register; it is read to the data outputs $Q_0 – Q_{17}$.

But, if $\overline{EMODE}$ is asserted (LOW), then the next 18-bit data word instead comes from the Control Register; it is read to the data outputs $Q_0 – Q_{17}$ at the third rising edge of RCLK. At the fourth rising edge of RCLK, reading again occurs from the Programmable-Almost-Empty-Flag-Offset-Value Register; and the same three-step reading sequence gets repeated on subsequent RCLK rising edges.

Reading contents from these two or ***three*** programmable registers does not have to occur all at one time, or to be effected by one single sequence of steps. Whenever $\overline{LD}$ is being asserted (is LOW) but $\overline{REN}$ is not being asserted (is HIGH), the FIFO's internal programmable-register-read-address pointer maintains its present value, without any reading actually taking place at each rising edge of RCLK. (See Table 3.) Thus, for instance, one or two programmable registers may be read, after which the FIFO may be returned to normal FIFO-array-read/write operation by deasserting $\overline{LD}$ (to HIGH).

To ensure correct operation, the simultaneous reading and writing of a register should be avoided.

FIRST LOAD/*RETRANSMIT ($\overline{FL}$/RT)*

$\overline{FL}$/RT is a dual-purpose signal. It is one of four input signals which select the grouping mode in which the FIFO operates after being reset; the other three of these input signals are ***$\overline{WXI}$/WEN_2***, ***$\overline{RXI}$/REN_2, and $\overline{EMODE}$. There are four*** possible grouping modes: standalone, ***interlocked paralleled***, cascaded 'master' or 'first-load,' and cascaded 'slave.' The designations 'master' and 'slave' pertain to IDT-compatible depth cascading. Tables 1 and 2 show the signal encodings which select each grouping mode.

In standalone or paralleled operation, the $\overline{FL}$/***RT*** pin should be grounded for strict IDT72215B/25B-compatible operation. ***However, if it is taken HIGH, regardless of the state of the $\overline{EMODE}$ control input, the FIFO's internal read-address pointer is reset to address the FIFO's first physical memory location, without the other usual reset actions being taken; in particular, the FIFO's internal write-address pointer is unaffected. Subsequent read operations may then again read out the same block of data, delimited by the FIFO's first physical memory location and the current value of the write pointer, as was read out previously. There is no limit on the number of times that a block of data may be retransmitted. The only restrictions are that neither the read-address pointer nor the write-address pointer may 'wrap around' and address the FIFO's first physical memory location a second time during the retransmission process, and that*** the retransmit facility is unavailable during cascaded operation.

In IDT-compatible cascaded operation, $\overline{FL}$/***RT*** is grounded for the 'master' or 'first-load' FIFO, to distinguish it from the other 'slave' FIFOs in the cascade, which must all have their $\overline{FL}$/***RT*** inputs HIGH during a reset operation. (See again Tables 1 and 2.) The cascade will not operate correctly either without any 'master' FIFO, or with more than one 'master' FIFO.

WRITE EXPANSION INPUT/*WRITE ENABLE 2 ($\overline{WXI}$/WEN_2)*

$\overline{WXI}$/***WEN_2*** is a dual-purpose signal. It is one of four input signals which select the grouping mode in which the FIFO operates after being reset; the other three of these input signals are $\overline{FL}$/***RT***, $\overline{RXI}$/***REN_2, and $\overline{EMODE}$***. There are ***four*** possible grouping modes: standalone, ***inter-***

BOLD ITALIC = Enhanced Operating Mode

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES (cont'd)

locked paralleled, cascaded 'master' or 'first-load,' and cascaded 'slave.' The designations 'master' and 'slave' pertain to IDT-compatible depth cascading. Tables 1 and 2 show the signal encodings which select each grouping mode.

In standalone operation, $\overline{WXI}$/***WEN2*** and $\overline{RXI}$/***REN2*** both must be grounded so that the FIFO comes up in the standalone grouping mode after a reset operation. ***In interlocked-paralleled operation, $\overline{WXI}$/WEN2 is tied to $\overline{FF}$ of the other paralleled FIFO, and $\overline{RXI}$/REN2 is tied to $\overline{EF}$ of that same other FIFO. This interconnection scheme ensures that both FIFOs will operate together, and remain coordinated, regardless of timing skews.***

In cascaded operation, $\overline{WXI}$/***WEN2*** is connected to the $\overline{WXO}$ (Write Expansion Output; actually $\overline{WXO}$/$\overline{HF}$) output of the previous FIFO in the cascade. $\overline{RXI}$/***REN2*** is likewise connected to the $\overline{RXO}$ (Read Expansion Output; actually $\overline{RXO}$/***$\overline{EF}$2***) output of that previous FIFO. A reset operation forces $\overline{WXO}$/$\overline{HF}$ and $\overline{RXO}$/***$\overline{EF}$2*** HIGH for each FIFO; consequently, all FIFOs with their $\overline{WXI}$/***WEN2*** and $\overline{RXI}$/***REN2*** inputs thus connected come up in one of the two cascaded grouping modes, according to whether their $\overline{FL}$/***RT*** inputs are grounded or tied HIGH. (See again Tables 1 and 2.)

READ EXPANSION INPUT/*READ ENABLE 2* ($\overline{RXI}$/*REN2*)

$\overline{RXI}$/***REN2*** is a dual-purpose signal. It is one of four input signals which select the grouping mode in which the FIFO operates after being reset; the other three of these input signals are $\overline{FL}$/***RT***, $\overline{WXI}$/***WEN2, and $\overline{EMODE}$***. There are *four* possible grouping modes: standalone, ***interlocked-paralleled***, cascaded 'master' or 'first-load,' and cascaded 'slave.' The designations 'master' and 'slave' pertain to IDT-compatible depth cascading. Tables 1 and 2 show the signal encodings which select each grouping mode.

In standalone operation, $\overline{WXI}$/***WEN2*** and $\overline{RXI}$/***REN2*** both must be grounded, so that the FIFO comes up in the standalone grouping mode after a reset operation. ***In interlocked-paralleled operation, $\overline{WXI}$/WEN2 is tied to $\overline{FF}$ of the other paralleled FIFO, and $\overline{RXI}$/REN2 is tied to $\overline{EF}$ of that same other FIFO. This interconnection scheme ensures that both FIFOs will operate together, and remain coordinated, regardless of timing skews.***

In cascaded operation, $\overline{RXI}$/***REN2*** is connected to $\overline{RXO}$ (Read Expansion Output; actually $\overline{RXO}$/***$\overline{EF}$2***)) of the previous FIFO in the cascade. $\overline{WXI}$/***WEN2*** is likewise connected to $\overline{WXO}$ (Write Expansion Output; actually $\overline{WXO}$/HF) output of that previous FIFO. A reset operation forces $\overline{RXO}$/***$\overline{EF}$2*** and $\overline{WXO}$/$\overline{HF}$ HIGH for each FIFO; consequently, all FIFOs with their $\overline{RXI}$/***REN2*** and $\overline{WXI}$/***WEN2*** inputs thus connected come up in one of the two IDT-compatible cascaded grouping modes, according to whether their $\overline{FL}$/***RT*** inputs are grounded or tied HIGH. (See again Tables 1 and 2.)

Data Outputs

DATA OUT ($Q_0 - Q_{17}$)

Data, programmable-flag-offset values, and ***Control-Register*** codes are output from the FIFO as 18-bit words on $Q_0 - Q_{17}$. Unused bit positions in offset-value words and ***Control-Register*** words are zero-filled.

Control/Status Outputs

FULL FLAG ($\overline{FF}$)

$\overline{FF}$ goes LOW whenever the FIFO is completely full. That is, whenever the FIFO's internal write pointer has completely caught up with its internal read pointer; so that, if another word were to be written, it would have to overwrite the unread word which is now in position for reading out by the next requested read operation. Under these conditions, the FIFO is filled to its nominal capacity, which is 512 18-bit words for the LH540215 or 1024 18-bit words for the LH540225 respectively. Write operations are inhibited whenever $\overline{FF}$ is LOW, regardless of the assertion or deassertion of Write Enable ($\overline{WEN}$).

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), $\overline{FF}$ initially is HIGH. But, whenever no read operations have been performed since the completion of the reset operation, $\overline{FF}$ goes LOW after 512 write operations for the LH540215, or after 1024 write operations for the LH540225. (See Table 4.)

$\overline{FF}$ gets updated after a LOW-to-HIGH transition of the Write Clock (WCLK).

PROGRAMMABLE ALMOST-FULL FLAG ($\overline{PAF}$)

$\overline{PAF}$ goes LOW whenever the FIFO is 'almost' full; that is, whenever subtracting the value of the FIFO's internal read pointer from the value of its internal write pointer yields a difference which is less than the value of the Programmable-Almost-Full-Flag Offset 'p.' The subtraction is performed using modular arithmetic, modulo the total nominal number of 18-bit words in the FIFO's physical memory, which is 512 for the LH540215 or 1024 for the LH540225 respectively.

The default value of 'p' after the completion of a reset operation is one-eighth of the total number of words in the FIFO-memory array, minus one: 63_{10} for the LH540215 or 127_{10} for the LH540225 respectively. However, 'p' may be set to any value which does not exceed this total nominal number of words for the device, as explained in the description of Load ($\overline{LD}$).

BOLD ITALIC = Enhanced Operating Mode

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), and no read operations have been performed since the completion of the reset operation, $\overline{PAF}$ goes LOW after (512-p) write operations for the LH540215, or after (1024-p) write operations for the LH540225. (See Table 4.)

If p is still at its default value, $\overline{PAF}$ is LOW whenever the FIFO is from seven-eighths full to completely full.

In the IDT-Compatible Operating Mode, $\overline{PAF}$ changes from HIGH to LOW only after a LOW-to-HIGH transition of the Write Clock WCLK, and from LOW to HIGH only after a LOW-to-HIGH transition of the Read Clock RCLK. Thus, in this operating mode, $\overline{PAF}$ behaves as an 'asynchronous flag.'

In the Enhanced Operating Mode, on the other hand, $\overline{PAF}$ gets updated only after a LOW-to-HIGH transition of the Write Clock WCLK, and thus behaves as a 'synchronous flag,' whenever Control Register bit 04 is HIGH. (See Table 5.)

WRITE EXPANSION OUT/HALF-FULL FLAG ($\overline{WXO}/\overline{HF}$)

$\overline{WXO}/\overline{HF}$ is a dual-purpose signal. In 'standalone' operation, it behaves as a Half-Full Flag ($\overline{HF}$), in accordance with Table 4. In IDT-compatible 'cascaded' operation, it behaves as a Write Expansion Output ($\overline{WXO}$) signal to coordinate writing operations with the next FIFO in the cascade. Under these same conditions, also, the dual-purpose $\overline{WXI}/$***WEN2*** and $\overline{RXI}/$***REN2*** inputs behave as Write Expansion Input ($\overline{WXI}$) and Read Expansion Input ($\overline{RXI}$) signals respectively.

When two or more LH540215 or LH540225 FIFOs are 'cascaded' to operate as a deeper 'effective FIFO,' in an IDT-style 'daisy-chain' ring configuration, the Write Expansion Input ($\overline{WXI}$) of each FIFO is connected to $\overline{WXO}$ of the previous FIFO in the ring, with $\overline{WXI}$ of the 'first-load' or 'master' FIFO being connected to $\overline{WXO}$ of the last FIFO so as to complete the ring. Similar connections are made for each FIFO in the ring, parallel to these $\overline{WXO}$-to-$\overline{WXI}$ connections, for Read Expansion Input ($\overline{RXI}$) and Read Expansion Output ($\overline{RXO}/$***EF2***, when it is behaving as $\overline{RXO}$).

When the last physical location has been written in a FIFO operating in cascaded mode, a LOW-going pulse is emitted by that FIFO on its $\overline{WXO}$ output, and the FIFO is deactivated for writing at the next valid WCLK; and the next FIFO in the ring is simultaneously activated for writing. Otherwise, $\overline{WXO}$ remains constantly HIGH whenever the FIFO is operating in cascaded mode. This LOW-going $\overline{WXO}$ pulse serves as a 'write token' in the 'token-passing' FIFO-cascading scheme; it is passed on to the next FIFO in the ring via its $\overline{WXI}$ input. When this next FIFO receives the write token, it is activated for writing at the next valid WCLK.

BOLD ITALIC = Enhanced Operating Mode

The foregoing description applies both to the 'first-load' or 'master' FIFO in the ring, and to any and all 'slave' FIFOs in the ring. However, $\overline{WXO}$ has no necessary function for FIFOs operating in the 'standalone' mode. Consequently, in that mode, the same output pin is used for $\overline{HF}$; it follows that $\overline{HF}$ is not available as an output from any FIFO which is operating in the IDT-compatible cascaded mode. A FIFO is initialized into 'cascaded master' mode, into 'cascaded slave' mode, ***into interlocked-paralleled mode***, or into standalone mode according to the state of its $\overline{WXI}/$***WEN2***, $\overline{RXI}/$***REN2***, and $\overline{FL}/$***RT*** control inputs during a reset operation, ***and of $\overline{EMODE}$***. (See Table 1, Table, 2, and Table 5.)

In standalone ***or interlocked-paralleled*** operation, $\overline{HF}$ goes LOW whenever the FIFO is more than half full; that is, whenever subtracting the value of the FIFO's internal read pointer from the value of its internal write pointer yields a difference which is less than half of the total nominal number of 18-bit words in the FIFO's physical memory, which is 256 for the LH540215 or 512 for the LH540225 respectively. (See Table 4.) The subtraction is performed using modular arithmetic, modulo this total nominal number of words, which is 512 for the LH540215 or 1024 for the LH540225 respectively.

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), and it is operating in standalone mode ***or in interlocked-paralleled*** mode, and no read operations have been performed since the completion of the reset operation, $\overline{HF}$ goes LOW after 257 write operations for the LH540215, or after 513 write operations for the LH540225. (See again Table 4.)

In the IDT-Compatible Operating Mode, $\overline{HF}$ changes from HIGH to LOW only after a LOW-to-HIGH transition of the Write Clock WCLK, and from LOW to HIGH only after a LOW-to-HIGH transition of the Read Clock RCLK. Thus, in this operating mode, $\overline{HF}$ behaves as an 'asynchronous flag.'

In the Enhanced Operating Mode, on the other hand, $\overline{HF}$ gets updated only after a LOW-to-HIGH transition of the Read Clock RCLK, or else after a LOW-to-HIGH transition of the Write Clock WCLK, according to the setting of bits 03 and 02 of the Control Register (see Table 5). Thus, in this mode $\overline{HF}$ behaves as a 'synchronous flag,' and may be synchronized either to the input side of the FIFO (i.e., to WCLK), or to the output side of the FIFO (i.e., to RCLK).

PROGRAMMABLE ALMOST-EMPTY FLAG ($\overline{PAE}$)

$\overline{PAE}$ goes LOW whenever the FIFO is 'almost empty'; that is, whenever subtracting the value of the FIFO's internal write pointer from the value of its internal read pointer yields a difference which is less than q + 1, where 'q' is the value of the Programmable-Almost-Empty-Flag Offset. The subtraction is performed using modular arithmetic, modulo the total nominal number of 18-bit words

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES (cont'd)

in the FIFO's physical memory, which is 512 for the LH540215 or 1024 for the LH540225 respectively.

The default value of q after the completion of a reset operation is one-eighth of the total number of words in the FIFO-memory array, minus one; 63 for the LH540215 or 127 for the LH540225 respectively. However, q may be set to any value which does not exceed this total nominal number of words for the device, as explained in the description of Load ($\overline{LD}$).

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), and no write operations have been performed since the completion of the reset operation, then $\overline{PAE}$ is LOW. (See Table 4.)

If q is still at its default value, $\overline{PAE}$ is LOW whenever the FIFO is from one-eighth full to completely empty.

In the IDT-Compatible Operating Mode, $\overline{PAE}$ changes from HIGH to LOW only after a LOW-to-HIGH transition of the Read Clock RCLK, and from LOW to HIGH only after a LOW-to-HIGH transition of the Write Clock WCLK. Thus, in this operating mode, $\overline{PAE}$ behaves as an 'asynchronous flag.'

In the Enhanced Operating Mode, on the other hand, $\overline{PAE}$ gets updated only after a LOW-to-HIGH transition of the Read Clock RCLK, and thus behaves as a 'synchronous flag,' whenever Control Register bit 01 is HIGH. (See Table 5.)

EMPTY FLAG ($\overline{EF}$)

$\overline{EF}$ goes LOW whenever the FIFO is completely empty. That is, whenever the FIFO's internal read pointer has completely caught up with its internal write pointer; so that, if another word were to be read out, it would have to come from the physical memory location which is now in position to be written into by the next requested write operation. Read operations are inhibited whenever $\overline{EF}$ is LOW, regardless of the assertion or deassertion of Read Enable ($\overline{REN}$).

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), and no write operations have been performed since the completion of the reset operation, then $\overline{EF}$ is LOW. (See Table 4.)

$\overline{EF}$ gets updated after a LOW-to-HIGH transition of the Read Clock RCLK.

READ EXPANSION OUT/*EMPTY FLAG 2* ($\overline{RXO}$/$\overline{EF_2}$)

$\overline{RXO}$/***$\overline{EF_2}$*** is a dual-purpose signal. In 'standalone' operation, it has no function. In IDT-compatible 'cascaded' operation, it behaves as a Read Expansion Output ($\overline{RXO}$) signal to coordinate writing operations with the next FIFO in the cascade. Under these same conditions, also, the dual-purpose $\overline{RXI}$/***REN_2*** and $\overline{WXI}$/***WEN_2*** inputs behave as Read Expansion Input ($\overline{RXI}$) and Write Expansion Input ($\overline{WXI}$) signals respectively.

When two or more LH540215 or LH540225 FIFOs are operating in IDT-compatible 'cascaded' mode as a deeper 'effective FIFO,' the dual-purpose $\overline{RXI}$/***REN_2*** and $\overline{WXI}$/***WEN_2*** inputs behave as Read Expansion Input ($\overline{RXI}$) and Write Expansion Input ($\overline{WXI}$) signals respectively. An IDT-style cascade of these FIFO devices has a 'daisy-chain' ring configuration; the Read Expansion Input ($\overline{RXI}$) of each FIFO is connected to $\overline{RXO}$ ($\overline{RXO}$/***$\overline{EF_2}$***, behaving as $\overline{RXO}$) of the previous FIFO in the ring, with $\overline{RXI}$ of the 'first-load' or 'master' FIFO being connected to $\overline{RXO}$ of the last FIFO so as to complete the ring. Similar connections are made for each FIFO in the ring, parallel to these $\overline{RXO}$-to-$\overline{RXI}$ connections, for Write Expansion Input ($\overline{WXI}$) and Write Expansion Output ($\overline{WXO}$).

When the last physical location has been read in a FIFO operating in IDT-style cascaded mode, a LOW-going pulse is emitted by that FIFO on its $\overline{RXO}$ output; otherwise, $\overline{RXO}$ remains constantly HIGH. This LOW-going $\overline{RXO}$ pulse serves as a 'read token' in the token-passing FIFO-cascading scheme; it is passed on to the next FIFO in the ring via its $\overline{RXI}$ input. When this next FIFO receives the read token, it is activated for reading at the next valid RCLK.

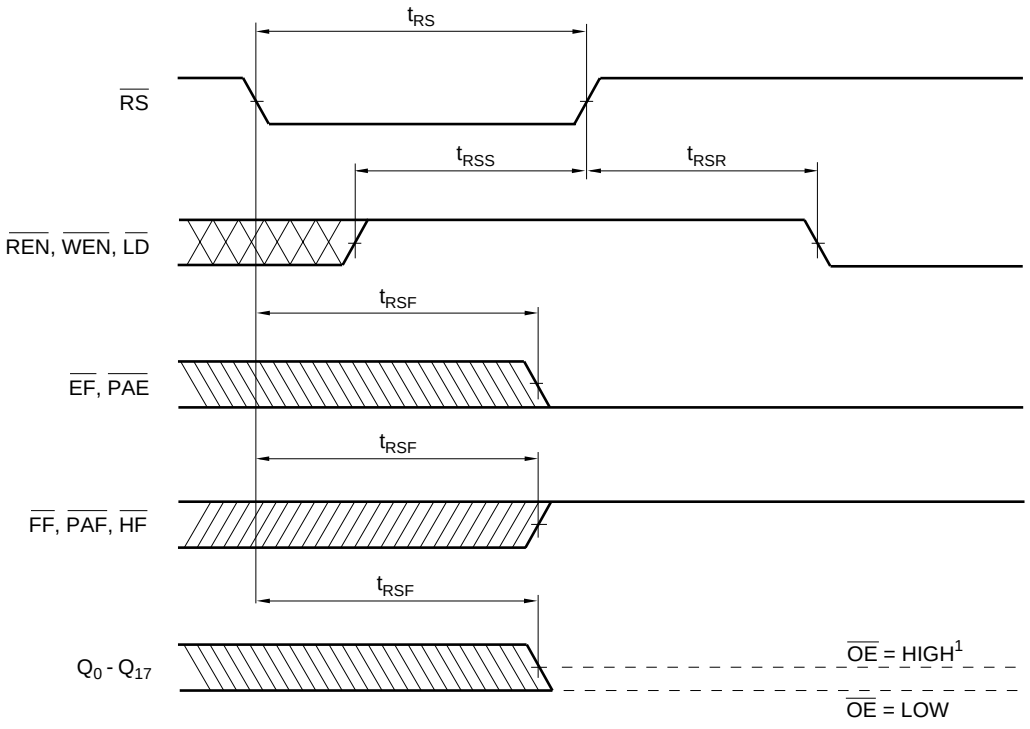
After a FIFO emits an $\overline{RXO}$ pulse, the FIFO is deactivated for reading at the next valid RCLK. Also, its data outputs go into high-Z state, regardless of the assertion or deassertion of its Output Enable ($\overline{OE}$) control input, until it again receives the token. Simultaneously, the next FIFO in the ring is activated for reading.

The foregoing description applies both to the 'first-load' or 'master' FIFO in the ring, and to any and all 'slave' FIFOs in the ring. However, $\overline{RXO}$ has no necessary function for a FIFO which is operating in 'standalone' mode. Consequently, in that mode, $\overline{RXO}$ is never asserted, and remains constantly HIGH. A FIFO is initialized into 'standalone' mode, into 'cascaded master' mode, or into 'cascaded slave' mode according to the state of its $\overline{WXI}$/***WEN_2***, $\overline{RXI}$/***REN_2***, and $\overline{FL}$/***RT*** control inputs during a reset operation. ***It also may be forced into interlocked-paralleled mode by $\overline{EMODE}$. (See Table 1, Table 2, and Table 5.)***

In the Enhanced Operating Mode, $\overline{RXO}$/$\overline{EF_2}$ behaves as a second Empty Flag $\overline{EF_2}$. $\overline{EF_2}$ is an exact duplicate of the main Empty Flag $\overline{EF}$, except that it is delayed with respect to $\overline{EF}$ by one full cycle of the Read Clock RCLK.

BOLD ITALIC = Enhanced Operating Mode

TIMING DIAGRAMS

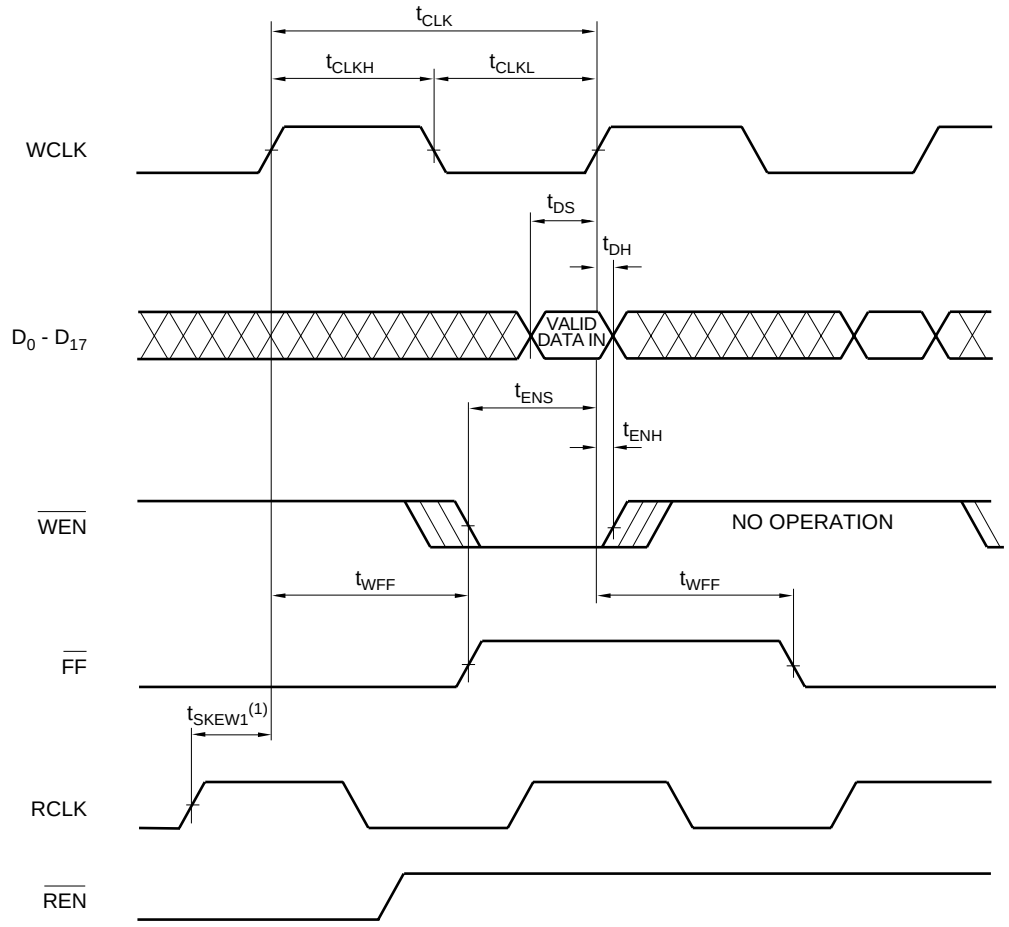


NOTES:
1. After reset, the outputs will be LOW if $\overline{OE}$ = LOW, and in a high-impedance state if $\overline{OE}$ = HIGH.
2. The clocks (RCLK, WCLK) may be free-running during a reset operation.

540215-5

Figure 6. Reset Timing

TIMING DIAGRAMS (cont'd)



NOTE:

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{FF}$ to change predictably during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then it is not guaranteed that $\overline{FF}$ will change state until the next following WCLK edge.

540215-6

Figure 7. Synchronous Write Operation

BOLD ITALIC = Enhanced Operating Mode

TIMING DIAGRAMS (cont'd)

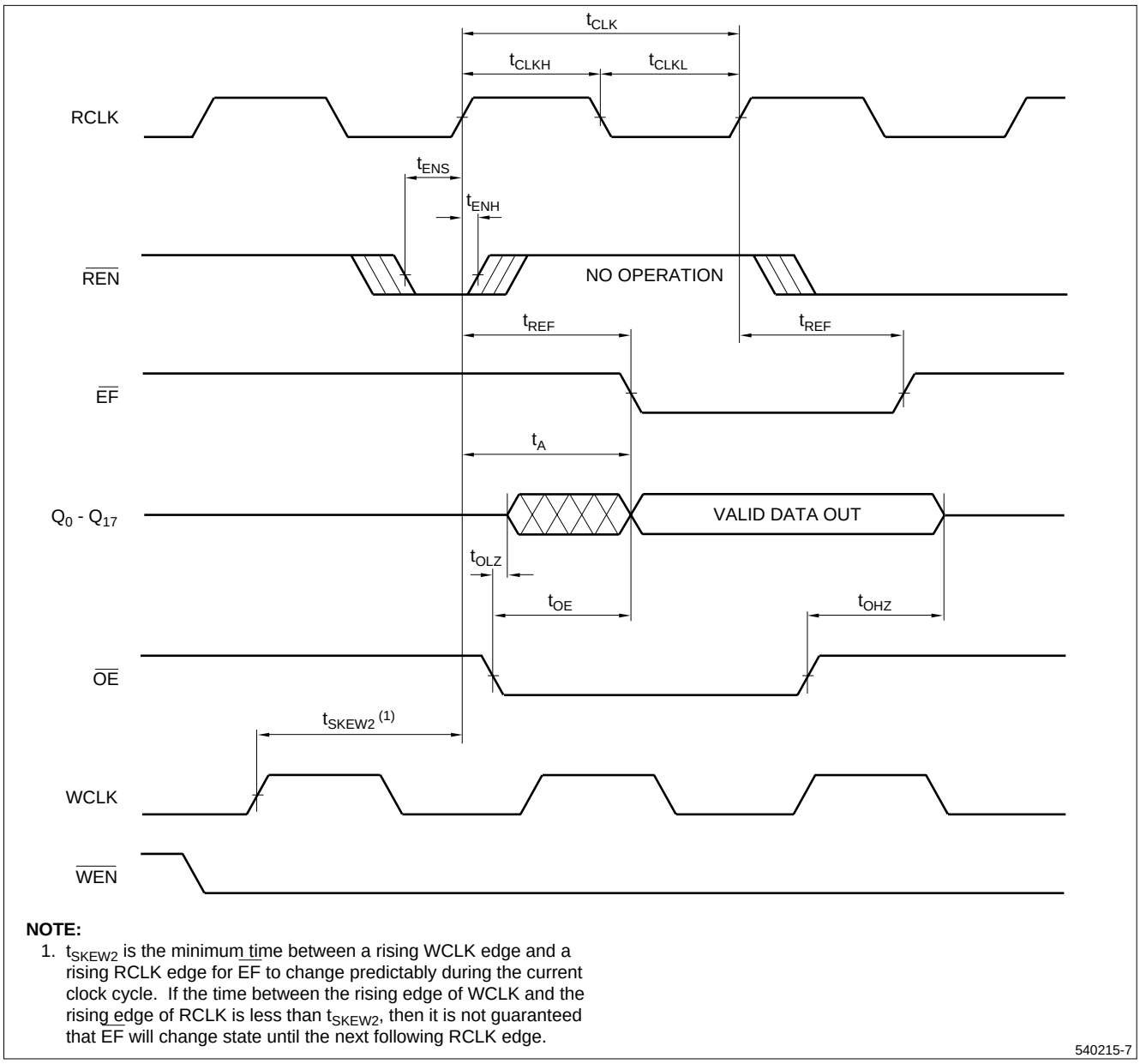
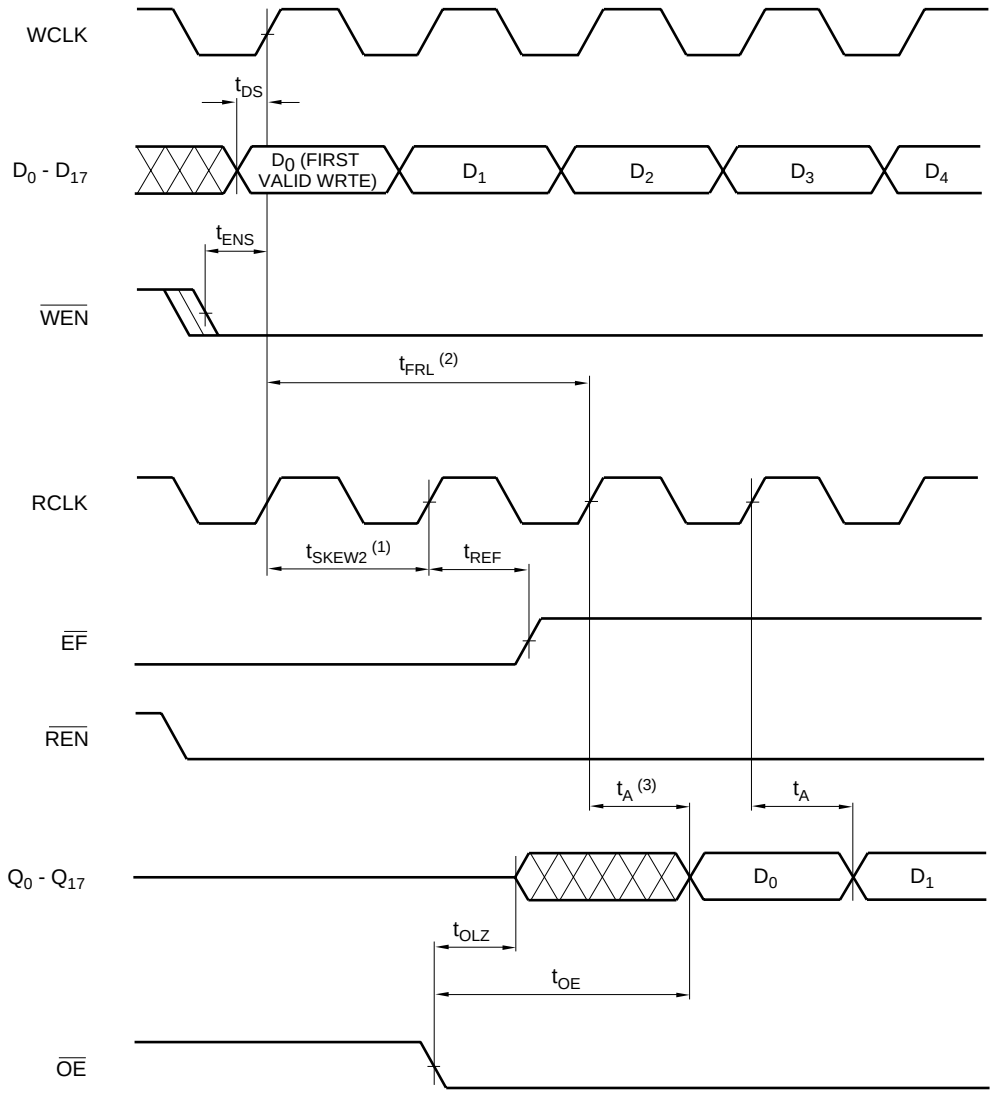


Figure 8. Synchronous Read Operation

TIMING DIAGRAMS (cont'd)



NOTES:

1. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{FF}$ to change predictably during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then it is not guaranteed that $\overline{FF}$ will change state until the next following WCLK edge.

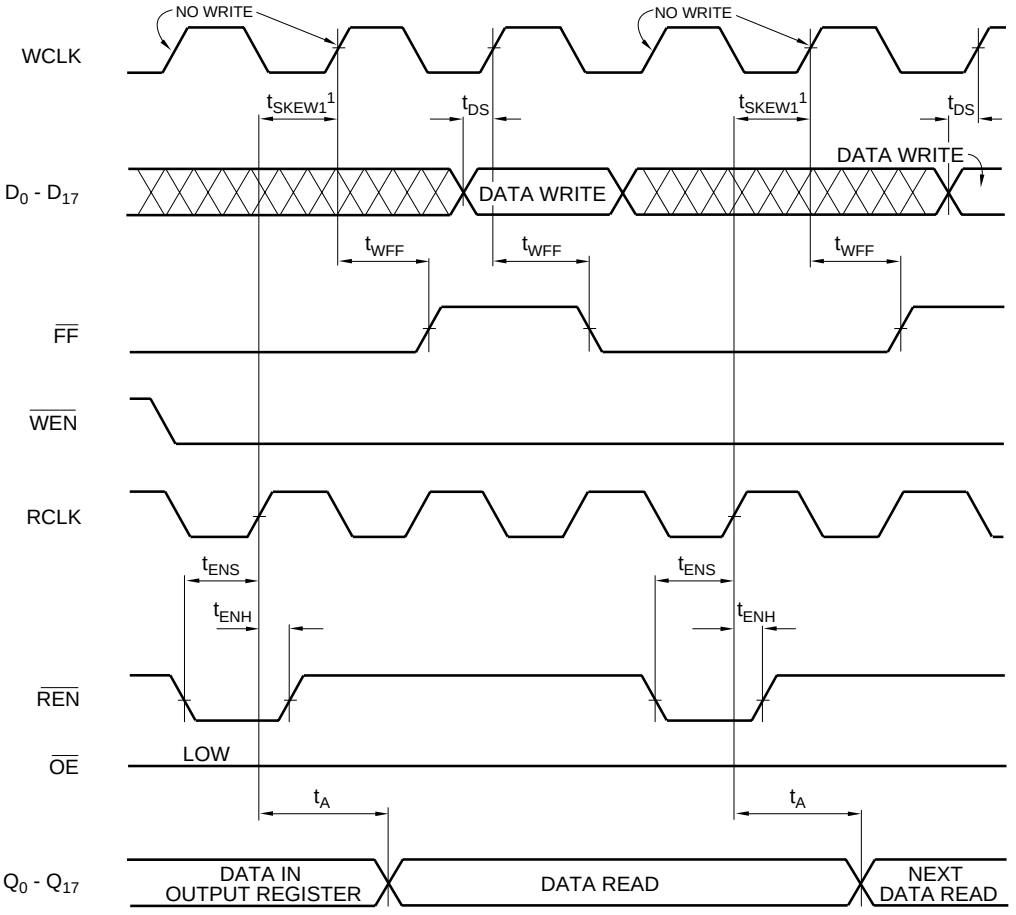
2. t_{FRL} (First-Read Latency) is the minimum time between a rising WCLK edge and a rising RCLK edge to assure a correct readout of the first data word D_0 in response to the next RCLK edge. Thus, $t_{FRL} = t_{CLK} + t_{SKEW2}$. If t_{FRL} is not met, D_0 may be available either at $t_{CLK} + t_{SKEW2}$, or after one more clock cycle delay at $2\ t_{CLK} + t_{SKEW2}$. The First-Read Latency timing restrictions apply only when the FIFO has been empty ($\overline{EF}$ = LOW).

3. $\overline{EF}$ may be used to determine when the first data word D_0 may be read. D_0 always is available on the next cycle after $\overline{EF}$ has gone HIGH.

540215-8

Figure 9. Latency for the First Data Word After a Reset Operation, With Simultaneous Read and Write

TIMING DIAGRAMS (cont'd)



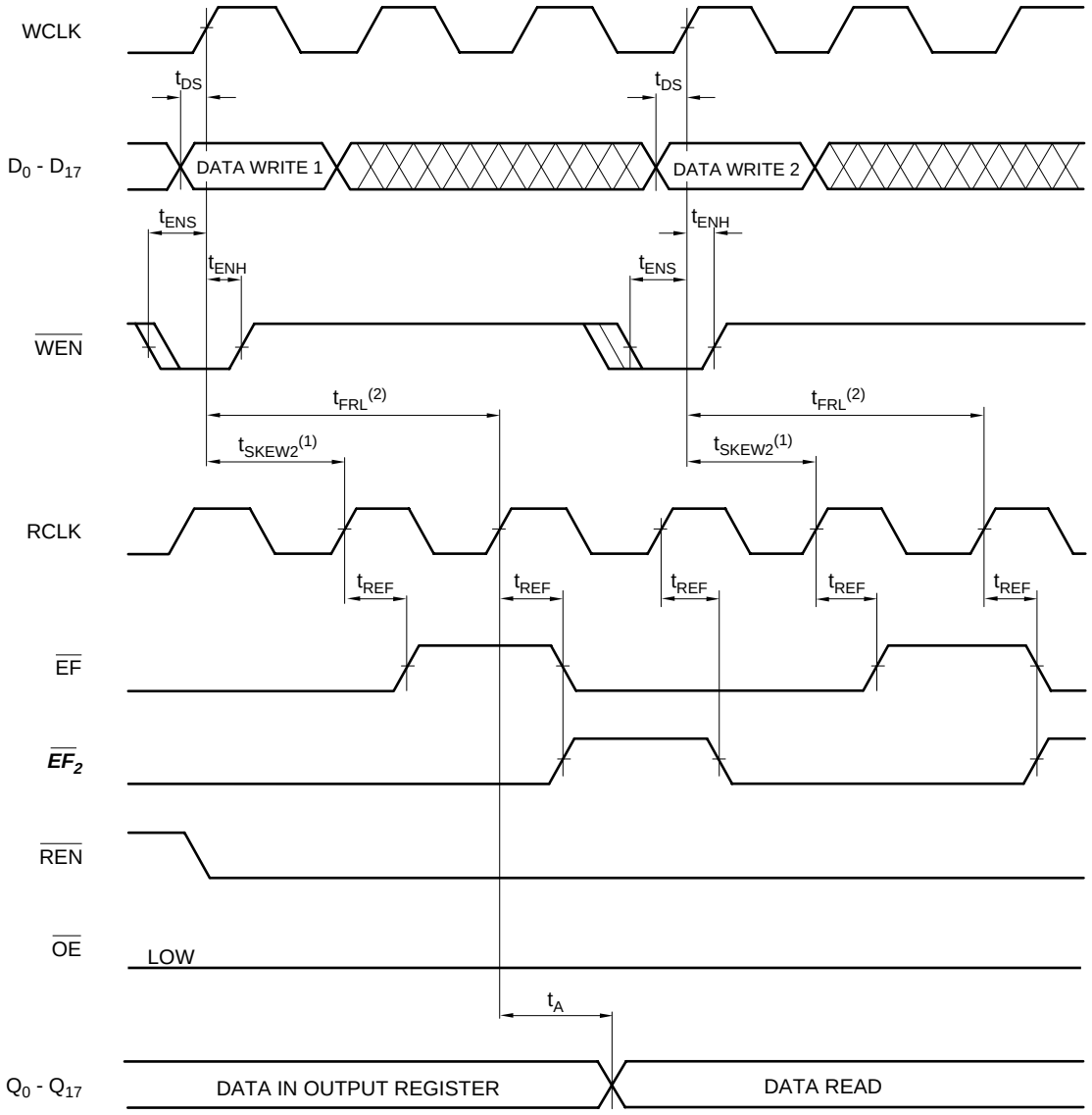
NOTE:

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for FF to change predictably during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then it is not guaranteed that FF will change state until the next following WCLK edge.

540215-9

Figure 10. Full-Flag Timing

TIMING DIAGRAMS (cont'd)



NOTES:

1. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{EF}$ to change predictably during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then it is not guaranteed that $\overline{EF}$ will change state until the next following RCLK edge.

2. t_{FRL} (First-Read Latency) is the minimum time between a rising WCLK edge and a rising RCLK edge to assure a correct readout of the first data word D_0 in response to the next RCLK edge. Thus, $t_{FRL} = t_{CLK} + t_{SKEW2}$. If t_{FRL} is not met, D_0 may be available either at $t_{CLK} + t_{SKEW2}$, or after one more clock cycle delay at 2 $t_{CLK} + t_{SKEW2}$. The First-Read Latency timing restrictions apply only when the FIFO has been empty ($\overline{EF}$ = LOW).

3. $\overline{EF}$ may be used to determine when the first data word D_0 may be read. D_0 always is available on the next cycle after $\overline{EF}$ has gone HIGH.

BOLD ITALIC = Enhanced Operating Mode.

540215-10

Figure 11. Empty-Flag Timing

TIMING DIAGRAMS (cont'd)

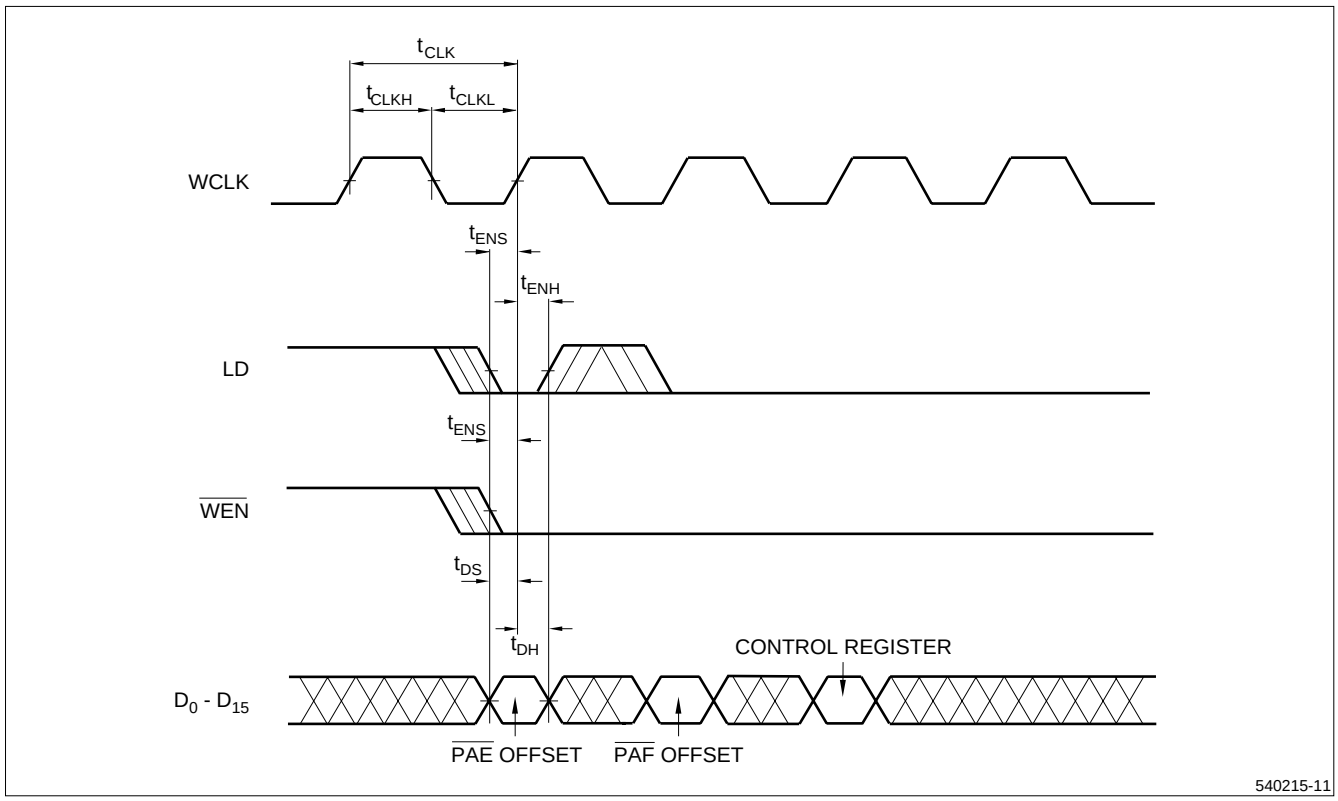


Figure 12. Programmable-Register Write Operation

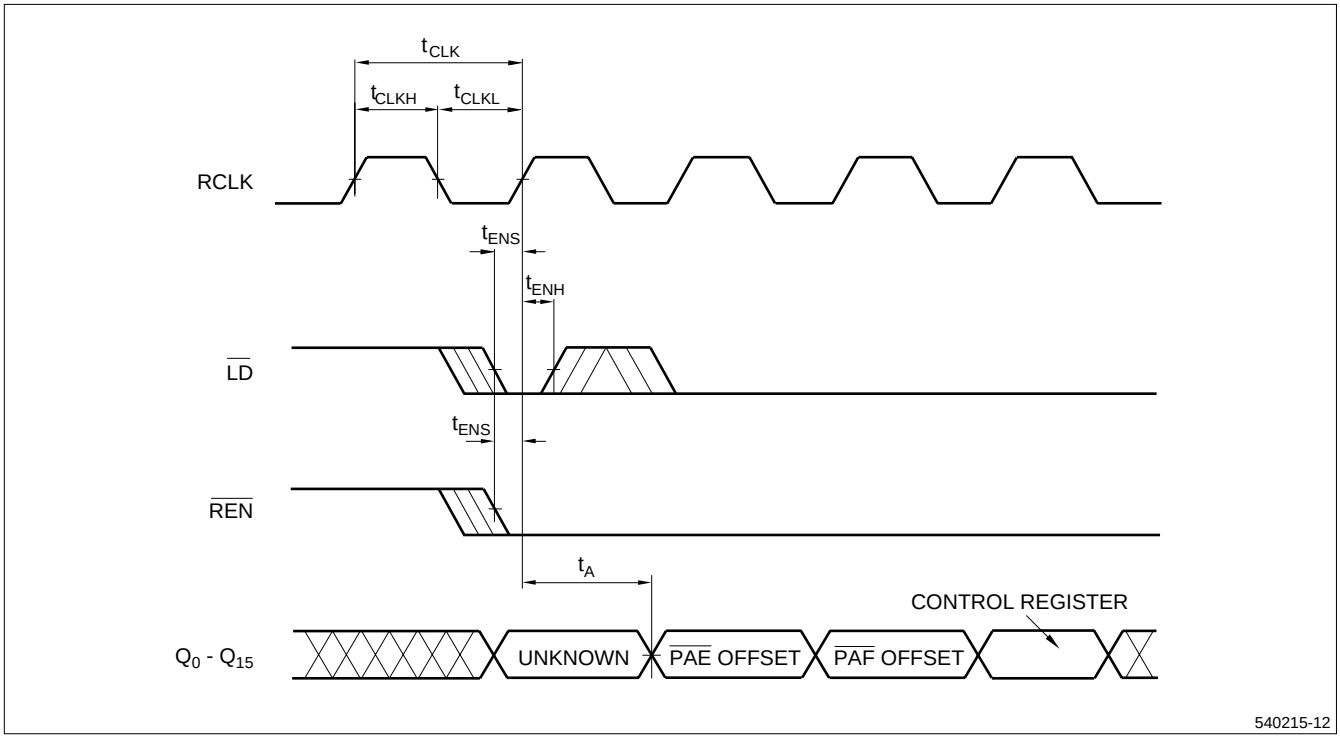
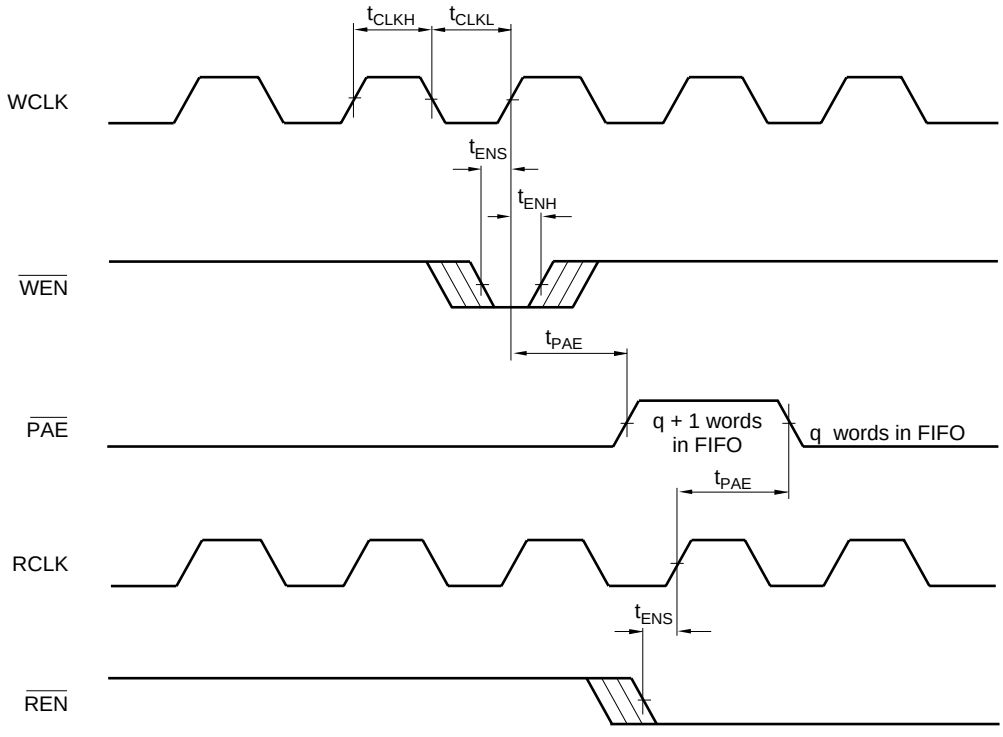


Figure 13. Programmable-Register Read Operation

TIMING DIAGRAMS (cont'd)



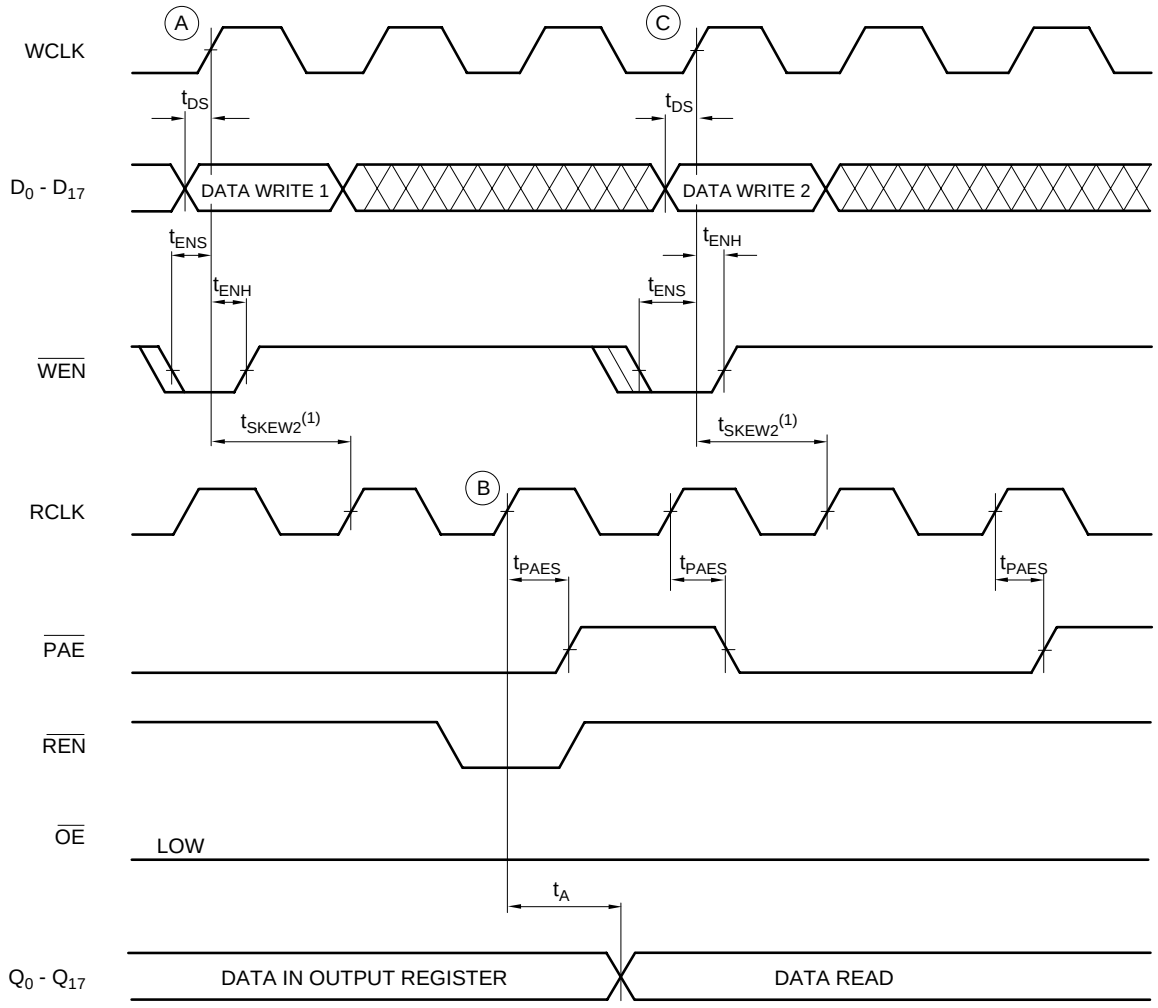
NOTE:
1. $\overline{PAE}$ offset = q. Also, number of data words written into FIFO already = q.

540215-13

Figure 14. Programmable-Almost-Empty Flag Timing, IDT-Compatible Operating Mode

TIMING DIAGRAMS (cont'd)

Enhanced Operating Mode Timing Diagram



NOTES:

1. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for PAE to change predictably during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then it is not guaranteed that PAE will change state until the next following RCLK edge.
2. PAE offset = q. Also, number of data words written into FIFO already = q.
3. The internal state of the FIFO:

   At (A), q+1 words.

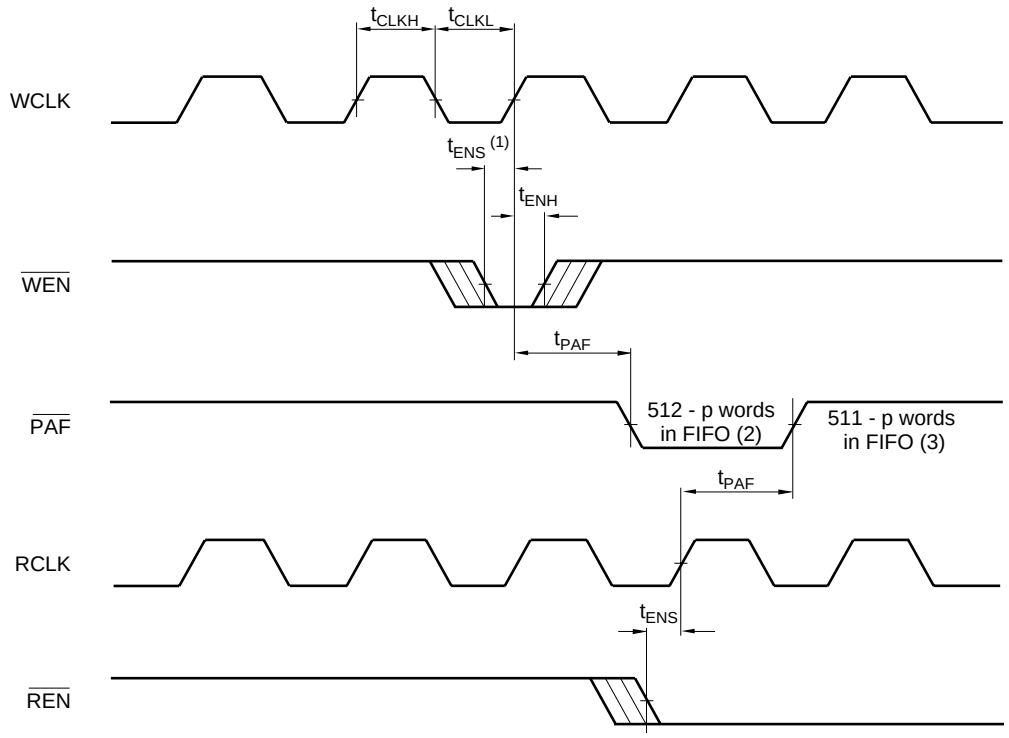
   At (B), q words.

   At (C), q+1 words again.

540215-23

Figure 15. Programmable-Almost-Empty Flag Timing, When Synchronous (Enhanced Operating Mode)

TIMING DIAGRAMS (cont'd)



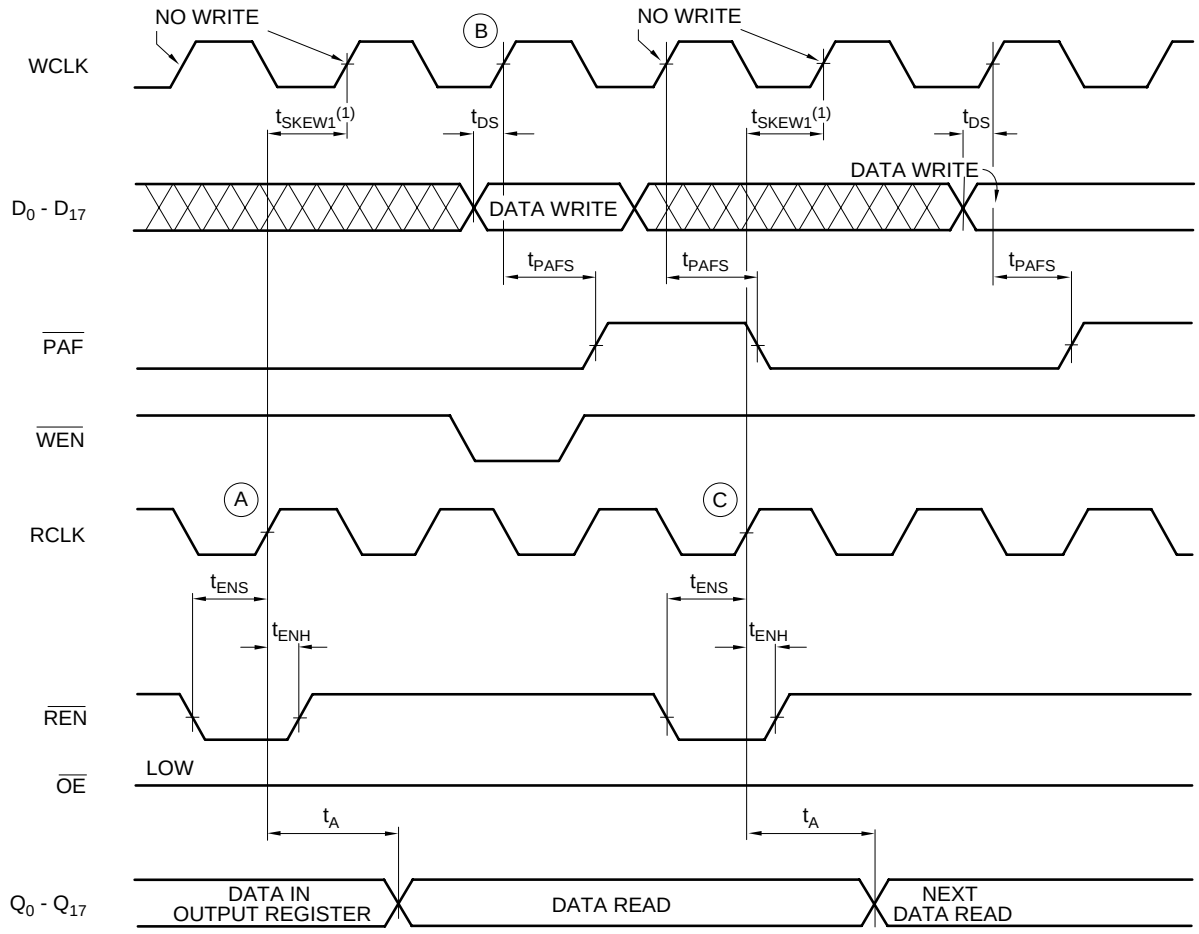
NOTES:
1. PAF offset = p. Number of data words written into FIFO already = 511 - p for the LH540215 and 1023 - p for the LH540225.
2. 512 - p words in FIFO for LH540215. 1024 - p words in FIFO for LH540225.
3. 511 - p words in FIFO for LH540215. 1023 - p words in FIFO for LH540225.

540215-14

Figure 16. Programmable Almost-Full-Flag Timing, IDT-Compatible Operating Mode

TIMING DIAGRAMS (cont'd)

Enhanced Operating Mode Timing Diagram



NOTES:

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for PAF to change predictably during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then it is not guaranteed that PAF will change state until the next following WCLK edge.
2. PAF offset = p. Number of data words written into FIFO already = 511 - p for the LH540215 and 1023 - p for the LH540225.
3. The internal state of the FIFO:

   At (A), 511 - p words in FIFO for LH540215 and 1023 - p words in FIFO for LH540225.

   At (B), 512 - p words in FIFO for LH540215 and 1024 - p words in FIFO for LH540225.

   At (C), again, 511 - p words in FIFO for LH540215 and 1023 - p words in FIFO for LH540225.

540215-24

Figure 17. Programmable-Almost-Full-Flag Timing, When Synchronous (Enhanced Operating Mode)

TIMING DIAGRAMS (cont'd)

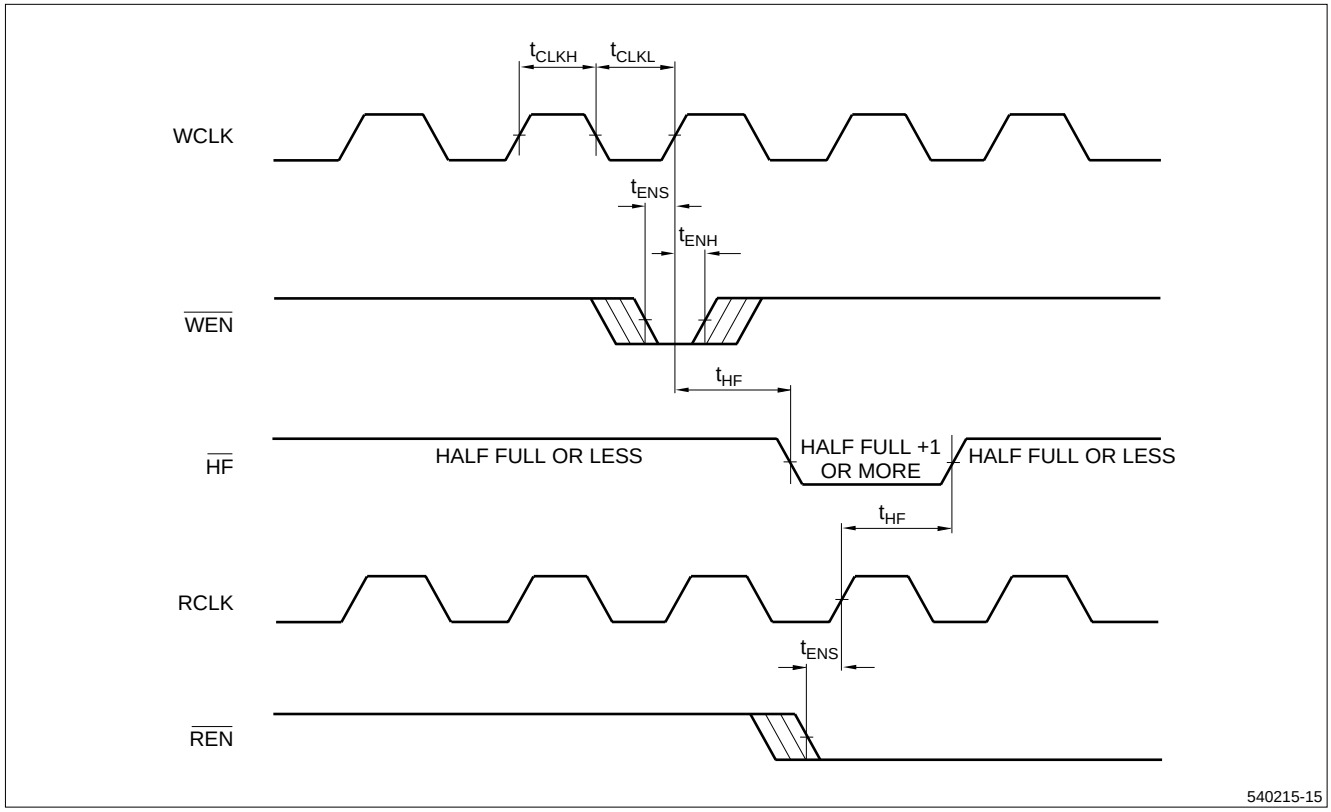
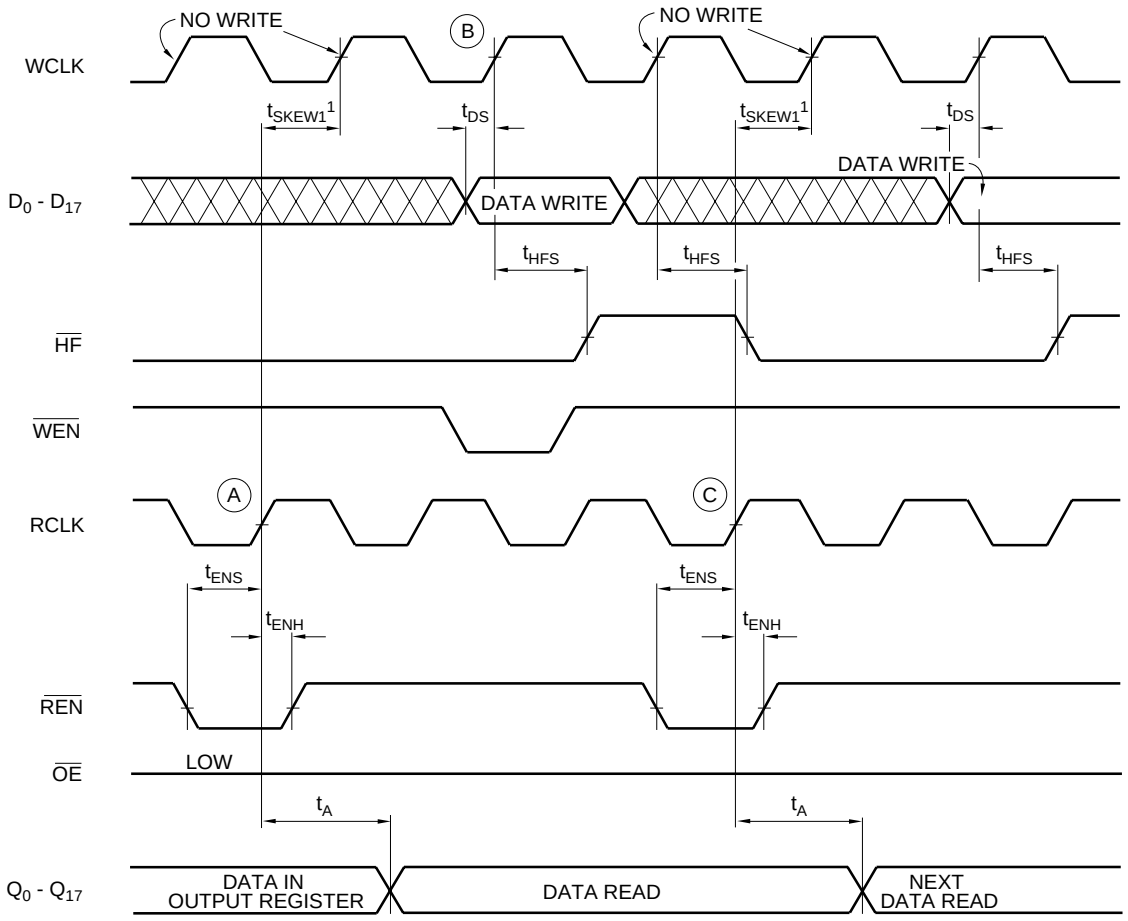


Figure 18. Half-Full-Flag Timing, IDT-Compatible Operating Mode

TIMING DIAGRAMS (cont'd)

Enhanced Operating Mode Timing Diagram



NOTES:

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{HF}$ to change predictably during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then it is not guaranteed that $\overline{HF}$ will change state until the next following WCLK edge.

2. The internal state of the FIFO:

   At (A), exactly half full.

   At (B), half+1 words.

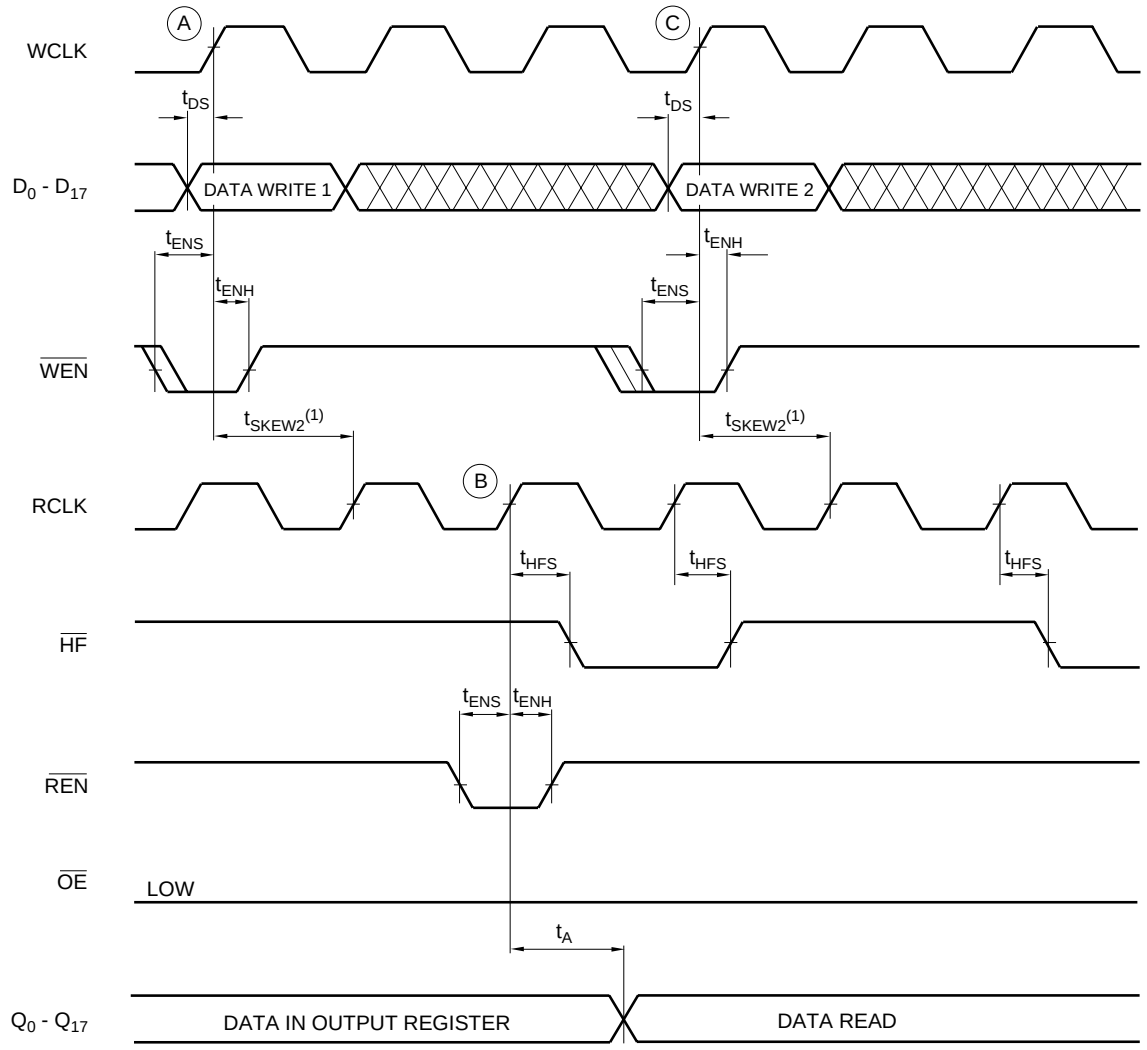
   At (C), exactly half full again.

540215-25

Figure 19. Half-Full-Flag Timing, When Synchronized to Input Port (Enhanced Operating Mode)

TIMING DIAGRAMS (cont'd)

Enhanced Operating Mode Timing Diagram



NOTE:

1. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{HF}$ to change predictably during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then it is not guaranteed that $\overline{HF}$ will change state until the next following RCLK edge.
2. The internal state of the FIFO:

   At (A), half+1 words.

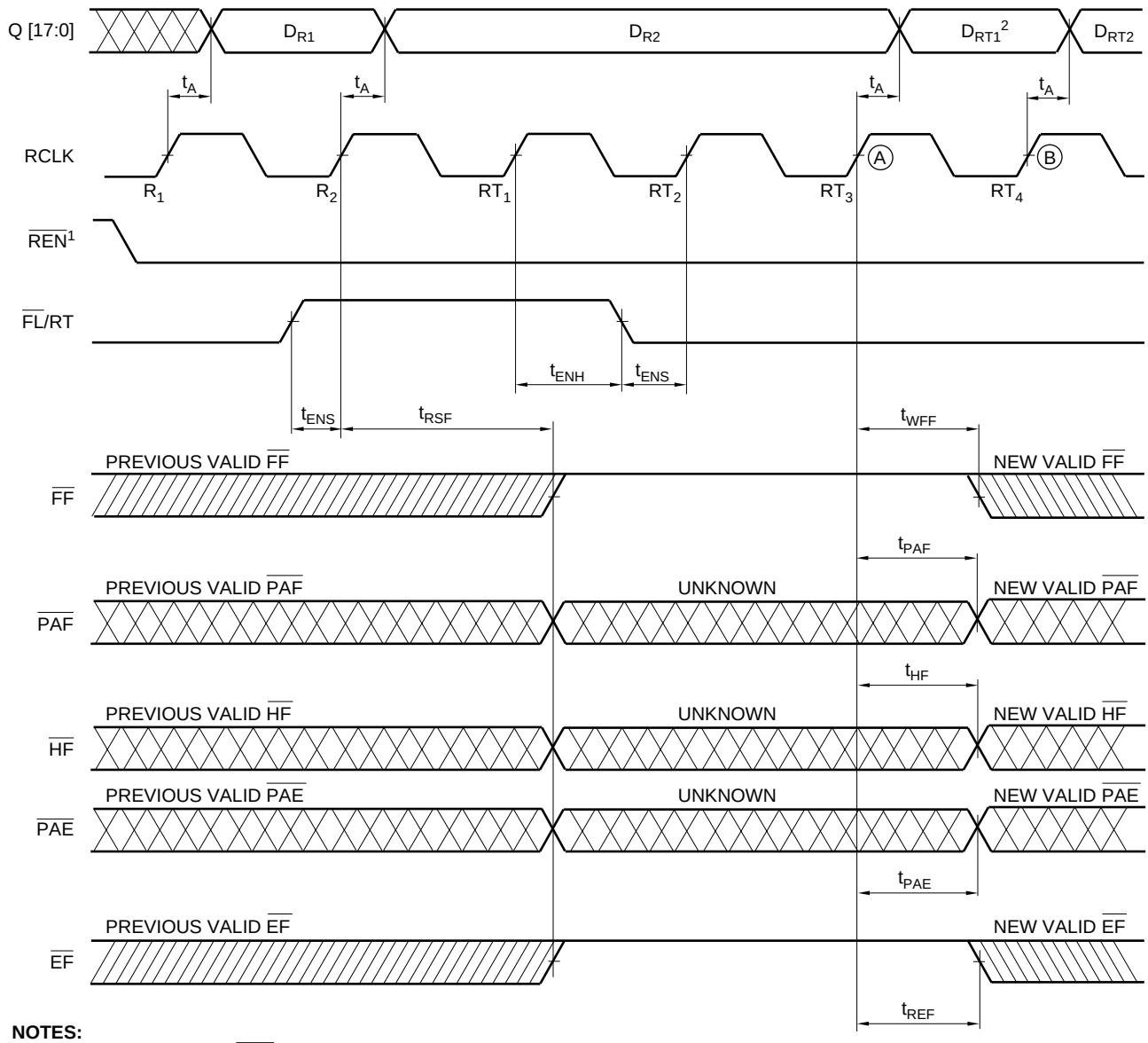
   At (B), exactly half full.

   At (C), half+1 words again.

540215-26

Figure 20. Half-Full-Flag Timing, When Synchronized to Output Port (Enhanced Operating Mode)

TIMING DIAGRAMS (cont'd)



NOTES:

1. It is not necessary for $\overline{REN}$ to be LOW for the device to recognize a retransmit request.
2. In order to actually read data words from the memory array, in IDT-Compatible Operating Mode, REN = LOW; ***in Enhanced Operating Mode, also REN_2 = HIGH (and $\overline{OE}$ = LOW, if Control Register bit 05 = HIGH).*** In any case, $\overline{LD}$ = HIGH.
3. D_{RT1} is the data item in physical location zero of the FIFO memory array.
4. The asynchronous intermediate flags (corresponding to LOW Control-Register bits) will show correct status three RCLK cycles after a retransmit operation, as is shown above. (RT_3, in the above RCLK waveform.)
5. The intermediate flags which have been synchronized to RCLK, by setting the appropriate Control-Register bits to HIGH will show correct status after (B), four RCLK cycles after a retransmit operation. (RT_4, in the above RCLK waveform.)
6. The intermediate flags which have been synchronized to WCLK, by setting the appropriate Control-Register bits HIGH, will show correct status on the second WCLK rising edge after (A), assuming that t_{SKEW1} was satisfied at (A); otherwise the flags will become valid on the third WCLK rising edge after (A).
7. Immediately after a reset operation, before any write operations have taken place, a retransmit operation is a 'no-op', and does not change the state of any FIFO registers or flags.
8. In the special case that the FIFO memory array contains **only one** valid data item, the status of $\overline{HF}$ and $\overline{PAF}$ should be ignored on a retransmit.

540215-28

Figure 21. Retransmit Timing

TIMING DIAGRAMS (cont'd)

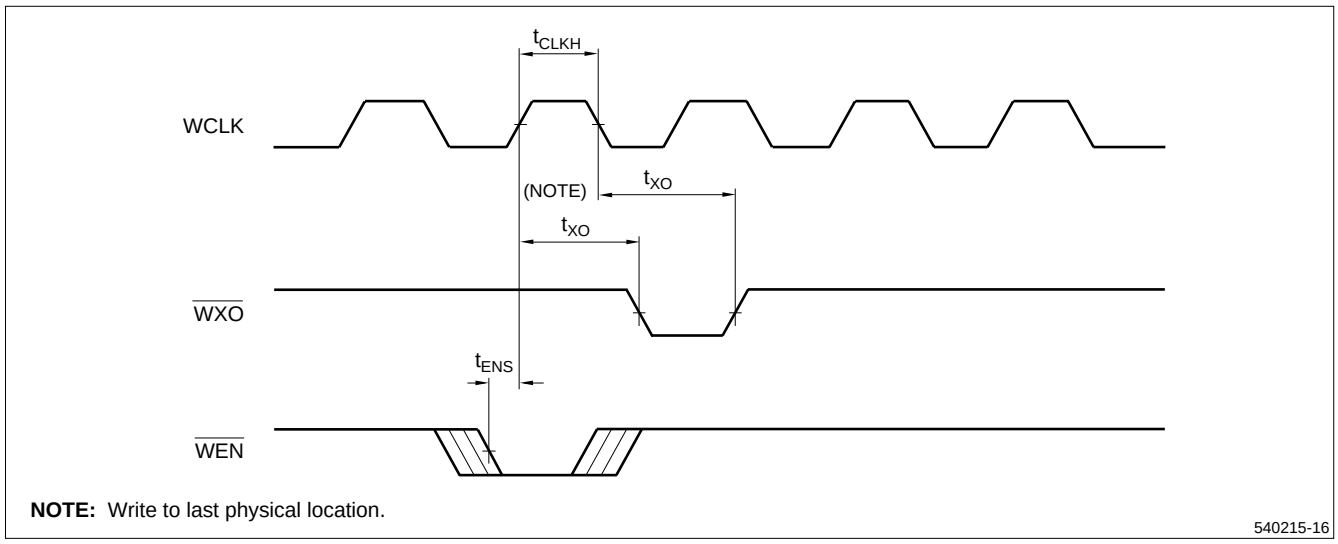


Figure 22. Write-Expansion-Out Timing, IDT-Compatible Operating Mode

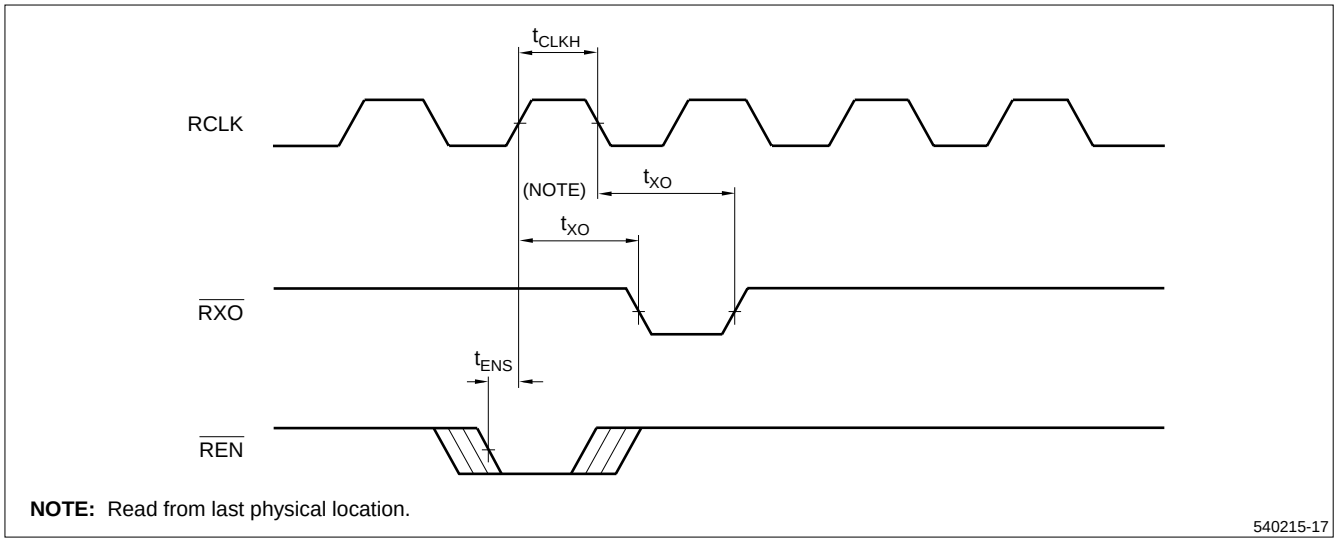


Figure 23. Read-Expansion-Out Timing, IDT-Compatible Operating Mode

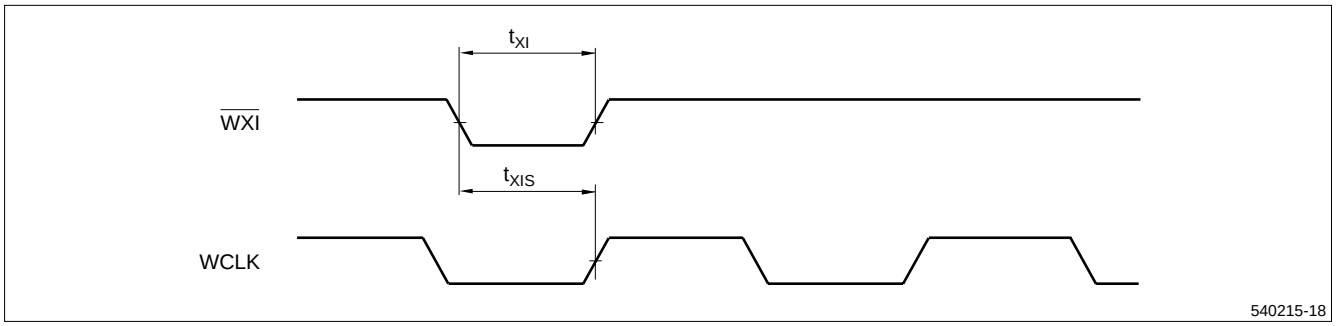


Figure 24. Write-Expansion-In Timing, IDT-Compatible Operating Mode

TIMING DIAGRAMS (cont'd)

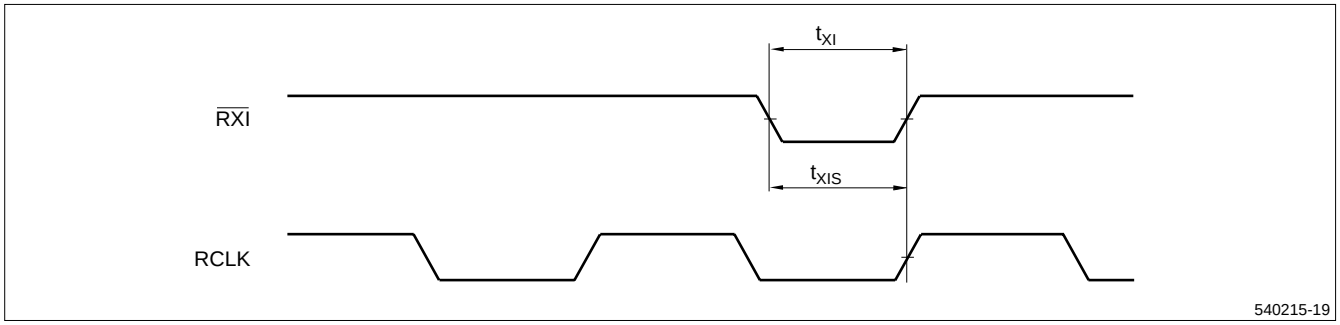


Figure 25. Read-Expansion-In Timing, IDT-Compatible Operating Mode

APPLICATIONS INFORMATION

Standalone Configuration

When depth cascading is not required for a given application, the LH540215/25 is placed in standalone mode by tying the two Expansion In pins $\overline{WXI}$/***WEN2*** and $\overline{RXI}$/***REN2*** to ground, while also holding the First Load/Retransmit pin $\overline{FL}$/***RT*** LOW for the duration of any reset operation. (See Table 1.) Subsequently, $\overline{FL}$/***RT*** may be taken HIGH at will, whenever a retransmit operation is desired. If not being used, $\overline{FL}$/RT also may be tied to ground, as shown in Figure 26.

Width Expansion

Word-width expansion is implemented by placing multiple LH540215/25 devices in parallel. Each device should be configured for standalone mode, unless the depth of one single FIFO is not adequate for the application. In this event, word-width expansion may in principle be used with either of the two depth-cascading schemes supported by the LH540215/25 architecture. In practice, the reliability benefits of interlocked-paralleled operation are available only with the pipelining scheme, making it the preferred alternative. (Refer to discussion in a later section.)

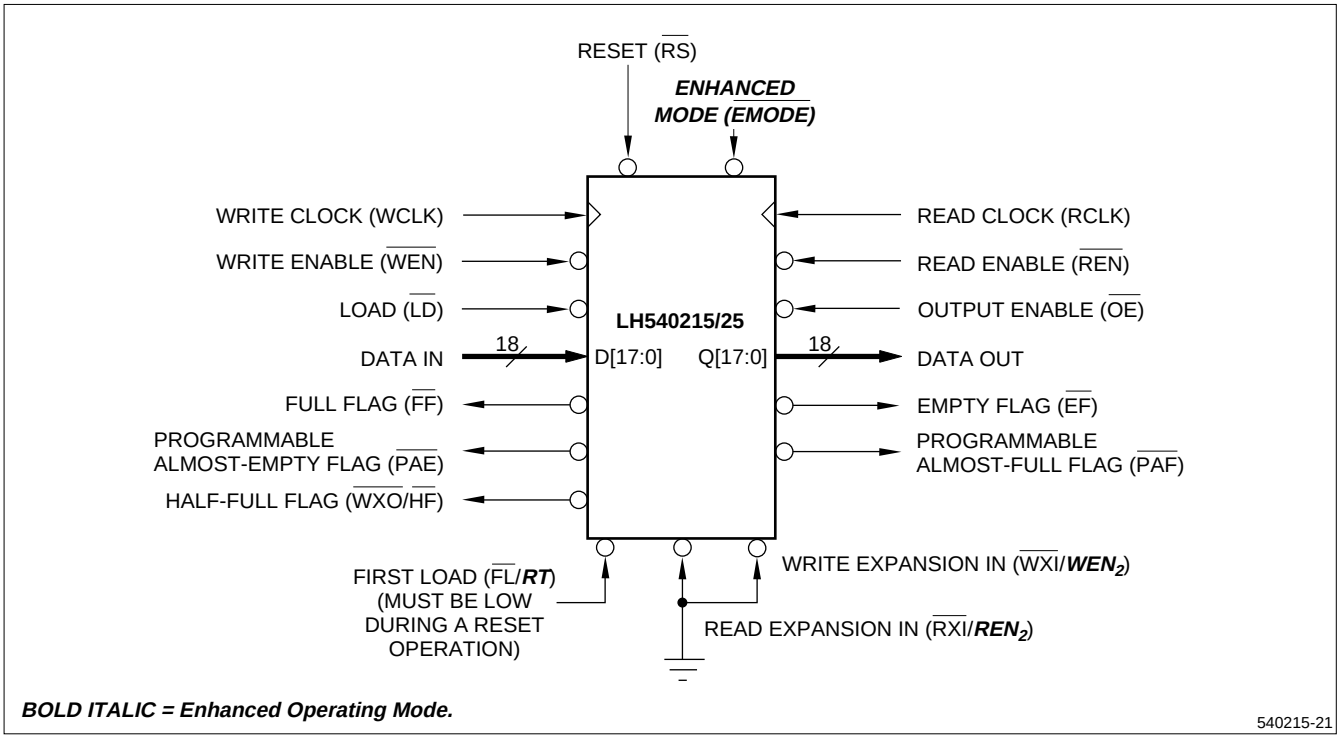


Figure 26. Standalone FIFO (512 × 18 / 1024 × 18)

BOLD ITALIC = Enhanced Operating Mode

When standalone-mode LH540215/25 devices are paralleled, the behavior of the status flags is identical for all devices; so, in principle, a representative value for each of these flags could be derived from any one device. In practice, it is better to derive 'composite' flag values using external logic, since there may be minor speed variations between different actual devices. After writing or reading have been in a disabled state, the process of re-enabling should be gated by the slowest FIFO.

For m paralleled FIFOs, the form of this external composite-flag logic may be an OR gate with m assertive-LOW inputs and an assertive-LOW output. In keeping with deMorgan's Theorem, such a gate may be implemented as an AND gate with m assertive-HIGH inputs and an assertive-HIGH output. Figure 27 illustrates the case m = 2.

The LH540215/25 architecture supports two very different methods of depth cascading:

Token passing, which follows the scheme used in the pin-compatible and functionally-compatible Integrated Device Technology IDT72205B/15B/25B/35B/45B FIFOs, which the LH540215/25 can directly replace.

Pipelining, which follows the scheme used in the Texas Instruments SN74ACT7801/11/81 FIFOs, and also in the Sharp LH543620 1024×36 FIFO. The SN74ACT7801/11/81 pinout closely resembles the LH540215/25 pinout, but is not identical.

Depth Cascading Using Token Passing

Using the token-passing approach, depth cascading is implemented by configuring the required number of LH540215/25s in a circular 'ring' fashion, with the Expansion Out outputs ($\overline{WXO}/\overline{HF}$ and $\overline{RXO}/\boldsymbol{\overline{EF_2}}$) of each device tied to the Expansion In inputs ($\overline{WXI}/\boldsymbol{\overline{WEN_2}}$ and $\overline{RXI}/\boldsymbol{\overline{REN_2}}$) of the next device. (See Figure 28.) Because a reset operation forces the $\overline{WXO}/\overline{HF}$ and $\overline{RXO}/\boldsymbol{\overline{EF_2}}$ outputs HIGH for each device, the $\overline{WXI}/\boldsymbol{\overline{WEN_2}}$ and $\overline{RXI}/\boldsymbol{\overline{REN_2}}$ inputs for the next device are HIGH during the reset operation; thus, these two inputs are HIGH for all devices in the ring. (See Tables 1 and 2, and also Figure 28.) All devices in the cascade must be in the IDT-Compatible Operating Mode; thus, their ***EMODE*** inputs must be tied to Vcc.

One FIFO in the cascade must be designated as the 'first-load' device, by tying its First Load input ($\overline{FL}/\boldsymbol{RT}$) to ground. All other devices must have their $\overline{FL}/\boldsymbol{RT}$ inputs tied HIGH. Under these circumstances, the Retransmit function is not available for use.

In this mode, the control inputs which govern writing (WCLK and $\overline{WEN}$) and the control inputs which govern reading (RCLK and $\overline{REN}$) are shared by all devices, while logic within each LH540215/25 governs the steering of data. The common Data Inputs of all devices are tied together; but only one LH540215/25 is enabled during any given write cycle. Likewise, the common three-state Data Outputs of all devices are wire-ORed together; but only one LH540215/25 is enabled, including its three-state outputs, during any given read cycle. A data word is handled only by one device as it passes through the cascade of FIFOs, regardless of how many FIFOs are being cascaded together.

In the token-passing depth-cascaded mode, external logic should be used to generate a composite Full Flag and a composite Empty Flag, by ANDing the $\overline{FF}$ outputs of all LH540215/25 devices together and by ANDing the $\overline{EF}$ outputs of all devices together, using AND gates with assertive-LOW inputs and an assertive-LOW output. Here, the meaning of these composite flags is direct: the cascade of FIFOs is full, if and only if all k FIFOs belonging to the cascade are individually full; and similarly for empty. In keeping with deMorgan's Theorem, these k-input assertive-LOW AND gates are implemented physically as k-input assertive-HIGH OR gates. Figure 28 illustrates the case k = 3.

Similar external logic also may be used to generate a composite Programmable Almost-Full Flag and a composite Programmable Almost-Empty Flag, by ANDing the $\overline{PAF}$ outputs of all LH540215/25 devices together and by ANDing the $\overline{PAE}$ outputs of all devices together. Here, however, some careful analysis is required, to determine exactly what the resulting composite flags mean. Their significance may vary widely, depending on the number of FIFOs in the cascade, and on the 'offset' values which are present in the offset registers for these FIFOs. More complex logical combinations of $\overline{PAF}$ outputs with $\overline{FF}$ outputs, and of $\overline{PAE}$ outputs with $\overline{EF}$ outputs, may be found useful in particular applications.

In any case, the Half-Full Flag and the Retransmit function are not available for devices being used in token-passing depth-cascaded mode.

BOLD ITALIC = Enhanced Operating Mode

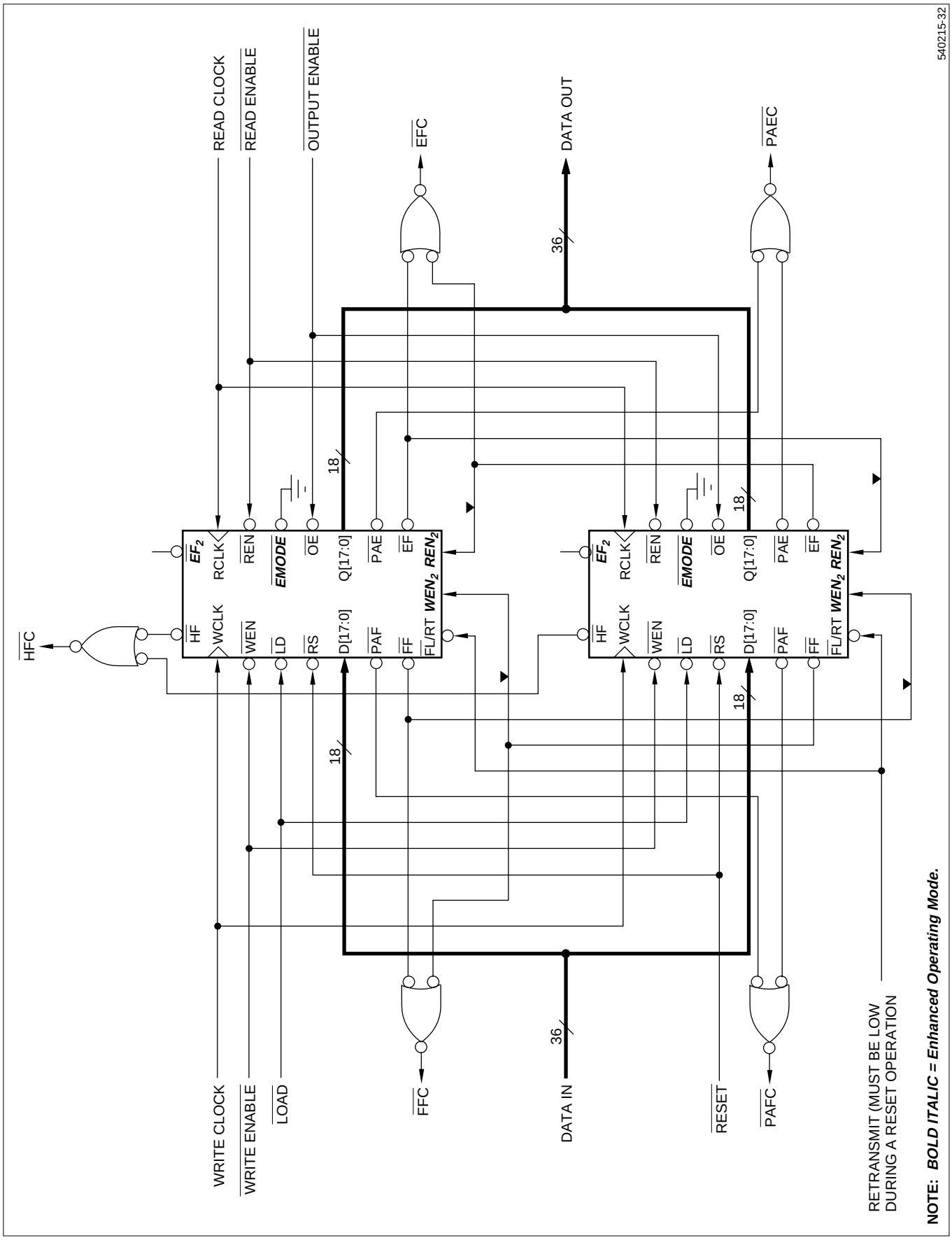
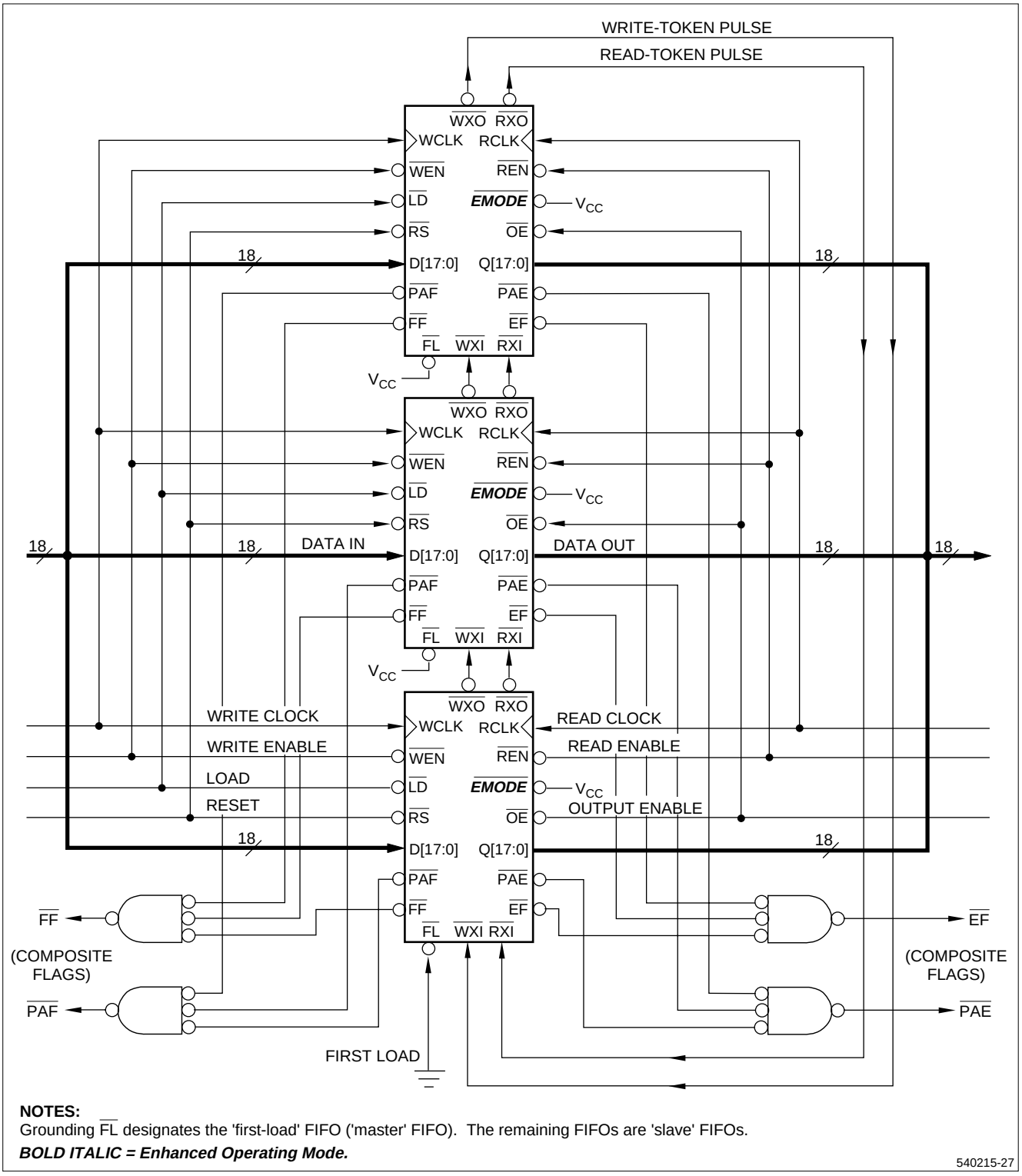


Figure 27. Interlocked-Paralleled Word-Width Expansion



NOTES:
Grounding $\overline{FL}$ designates the 'first-load' FIFO ('master' FIFO). The remaining FIFOs are 'slave' FIFOs.
BOLD ITALIC = Enhanced Operating Mode.

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Figure 28. Synchronous-FIFO Depth-Cascading Using IDT-Compatible 'Token-Passing' Scheme

Depth Cascading Using Pipelining

Using the pipelining approach, depth cascading is implemented by connecting the required number of LH540215/25s in series. Within the cascade, the Data Outputs of each device are connected to the Data Inputs of the next device. (See Figure 29a.) All devices in the cascade must be in ***the Enhanced Operating Mode***; thus, their ***$\overline{EMODE}$*** inputs must be grounded.

Successive devices in the cascade are crosscoupled; they control each other, using a 'handclasp' scheme for crossconnecting their control inputs and their status outputs. (See again Figure 29a.) The input side of the first device, and the output side of the last device, are not crosscoupled to other devices. Their control/status and clock pins are connected to the external system.

For the FIFO devices within the cascade, transferring data from each device to the next device is governed by a clock. Preferably, the same clock should be used at every FIFO-to-FIFO data-transfer interface boundary within the cascade. This 'Transfer Clock' may be either the external Write Clock, or the external Read Clock. If both of these two clocks are periodic and free-running, the faster of the two is the obvious choice for the 'Transfer Clock.' Of course, in principle, the 'Transfer Clock' may even be some other, totally-different clock.

The Empty Flag of each device is used to govern writing into the next device, and the Full Flag of each device is used to govern reading from the preceding device. Since the standard Empty Flag $\overline{EF}$ occurs one RCLK cycle too early to properly enable/disable the next device, ***the duplicate Empty Flag $\overline{EF_2}$ is used instead; $\overline{EF_2}$ is an exact copy of $\overline{EF}$, except that it is delayed by one full RCLK cycle with respect to $\overline{EF}$.***

Also, since the usual enable signals $\overline{WEN}$ and $\overline{REN}$ have the wrong polarity to function properly in this 'handclasp' mode, they are grounded for all devices within the cascade. ***The duplicate but inverted signals WEN_2 and REN_2 are used instead.***

$\overline{EF_2}$, WEN_2, and REN_2 are available only in Enhanced Operating Mode. They share the same pins which in IDT-Compatible Operating Mode are used respectively for $\overline{RXO}$, $\overline{WXI}$, and $\overline{RXI}$. Hence, for pipelined operation, all devices in the cascade must be in the Enhanced Operating Mode; their $\overline{EMODE}$ control inputs must be grounded.

When all of the foregoing conditions have been met in the interconnection of the pipelined array, then: At each device-to-device interface boundary within the array, a data word is transferred from the upstream device to the downstream device after *every* transfer-clock rising edge, as long as the upstream device is not empty and the downstream device is not full.

There is one possible anomalous behavior, which can occur if at any time the device upstream from a FIFO-to-FIFO boundary ('device n-1') becomes totally empty, at the same time as the downstream device ('device n') becomes totally full. Under these relatively-infrequent conditions, one extra copy of the last word transferred out of device n-1, which remains still available at the outputs of that device, gets introduced into the data stream. The simple circuit illustrated in Figure 29b avoids introducing this extra word, and does not slow down the operation of the pipeline if it is implemented with logic which is sufficiently fast. Table 6 indicates the speed requirements for this circuit which correspond to the various speed grades of LH540215/25. If the infrequent introduction of such an extra word is not of concern for a given cascaded-LH540215/25 application, the circuit of Figure 29b may safely be omitted.

Table 6. Required External-Logic Speeds for Pipelined Depth-Cascading Operation at Maximum Rate of Speed Grade

	SPEED GRADE (CYCLE TIME)		
	20 ns	**25 ns**	**35 ns**
Ta	≤ 8 ns	≤ 10 ns	≤ 15 ns
Tb	≤ 15 ns	≤ 19 ns	≤ 28 ns

NOTES:
1. Ta is the setup time for the signal '$\overline{FF}$ (DEVICE n),' including the delay of the assertive-LOW AND gate, with respect to the clock.
2. Tb is the clock-to-output time for the signal 'WEN_2 (DEVICE n),' including the delay of the assertive-HIGH AND gate.

Two PLDs (Programmable Logic Devices) suffice to implement the circuit of Figure 29b ten times, which allows for the cascading of LH540215/25s eleven deep. The choice of a GAL20RA10B-10 PLD to implement the flipflop and the two AND gates at its inputs, and a GAL22V10C-5 PLD to implement the simple AND gate which follows the flipflop, provides a sufficiently fast circuit to allow a cascade of LH540215/25-20 devices (the fastest speed grade presently offered by Sharp) to operate with no speed degradation. Designers experienced in using PLDs may recognize other implementations.

BOLD ITALIC = Enhanced Operating Mode

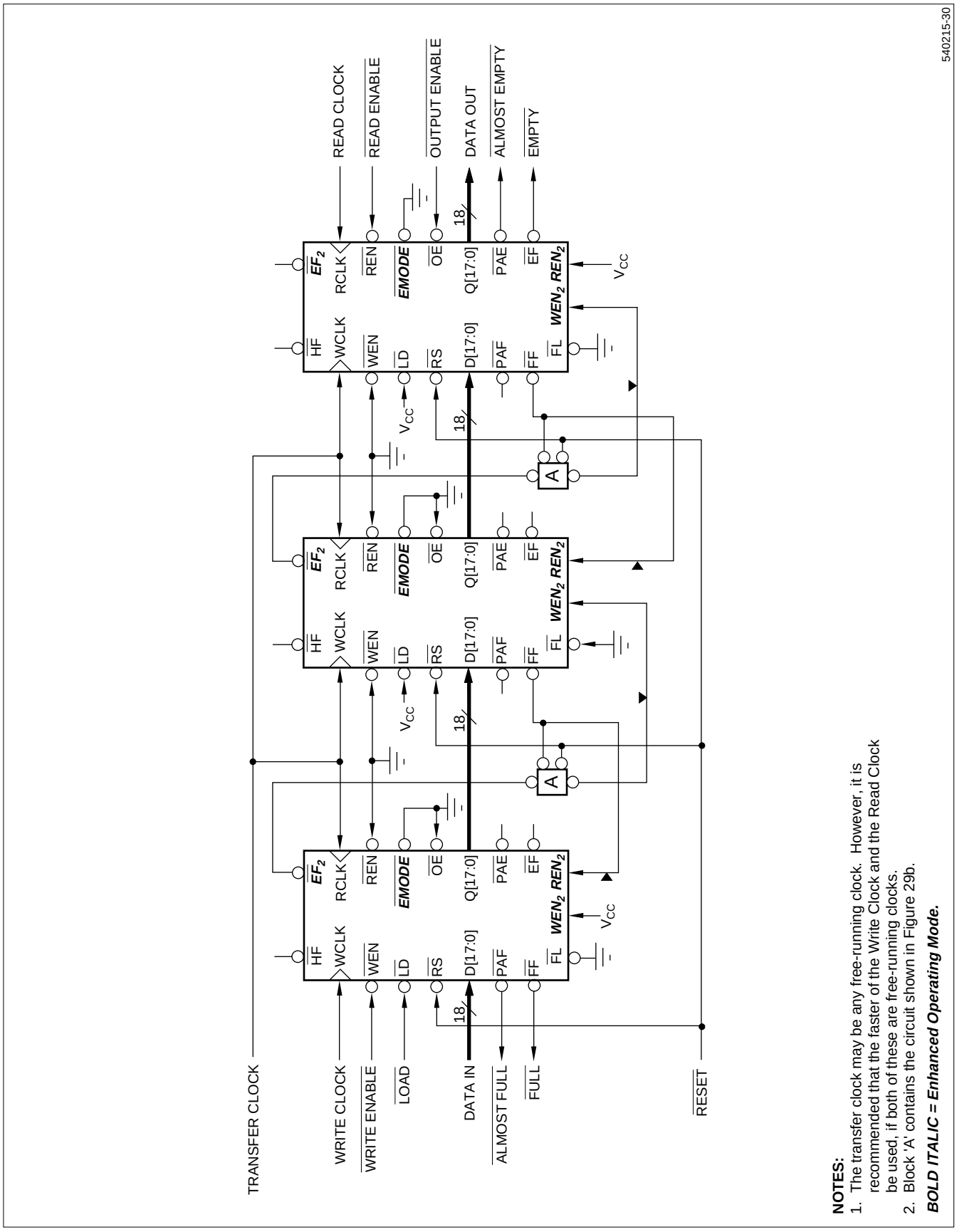
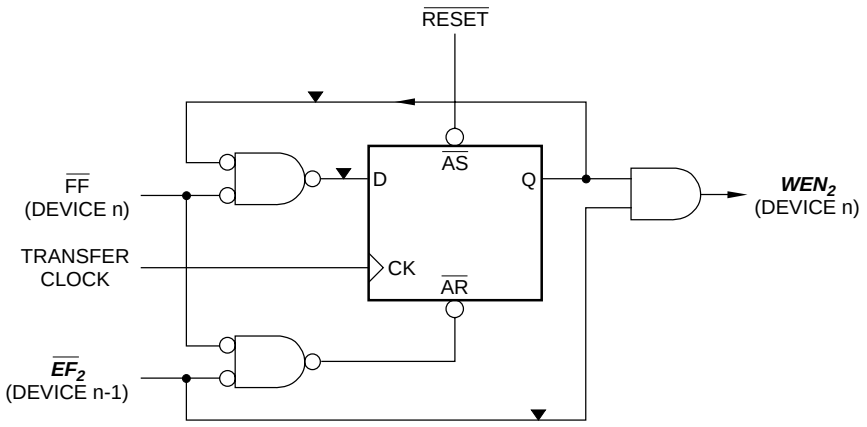


Figure 29a. TI-Style Pipelined Depth-Cascading



NOTES:
1. AS sets Q=1 regardless of CK or D. (Asynchronous Set.) AR sets Q=0 regardless of CK or D. (Asynchronous Reset.)
2. Q=0 occurs if and only if device n-1 goes completely empty and device n goes completely full. Q=0 is maintained as long as these conditions persist.
3. This circuit is used as block 'A' in Figure 29a and in Figure 30.

BOLD ITALIC = Enhanced Operating Mode.

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Figure 29b. External Logic Needed for TI-Style Pipelined Depth Cascading

The GAL20RA10B and GAL22V10C PLDs each provide ten macrocells. One macrocell may be configured to operate as a simple inverting or non-inverting buffer, a simple NAND or AND gate, an AND-OR gate, or a flipflop with an AND-OR input structure. The GAL20RA10B macrocell architecture in particular supports the implementation of an asynchronous-set/reset clocked D flipflop like the one shown in Figure 29b, except for some polarity differences at certain points within the logic diagram. If a slower implementation of the final AND gate can be tolerated in a given application, a single GAL20RA10B may be used to implement the circuit of Figure 29b five times, thus allowing for a cascade six FIFOs deep, with no second PLD being necessary. The GAL20RA10B and GAL22V10C PLDs are manufactured by Lattice Semiconductor Corporation, 5555 Northeast Moore Court, Hillsboro, OR 97124, USA.

Width Expansion Along With Depth Cascading

In principle, width expansion may be used with either of the two possible depth-cascading schemes.

However, when using the token-passing depth-cascading scheme, width expansion reduces simply to placing two or more cascades in parallel. In this mode of interconnection, no architectural support is available for interlocked-paralleled operation. Composite-flag logic may, of course, be designed to fit any complete array configuration, to determine meaningful full and empty indications for the entire array. This logic may, for instance, OR the $\overline{FF}$ and $\overline{EF}$ signals from the devices at the same relative position in each of the paralleled cascades, and then AND all of the rank-$\overline{FF}$ signals together; and likewise for all of the rank-$\overline{EF}$ signals. Then, the entire array is indicated to be full, if all ranks of devices (across the paralleled cascades) are individually full; and, similarly for empty.

When using the pipelined depth-cascading scheme, on the other hand, the first rank of devices (the one which receives input data words from the external system) and the last rank of devices (the one which provides output data words to the external system) may be operated in an interlocked-paralleled manner. Figure 30 shows a suggested interconnection scheme for two paralleled cascades, each three devices deep. The entire array of Figure 30 would comprise a 3072×36 'effective FIFO,' if implemented with 1024×18 LH540225 devices. Whenever the number of paralleled cascades exceeds two, a small amount of external logic is necessary to implement the interlocking.

BOLD ITALIC = Enhanced Operating Mode

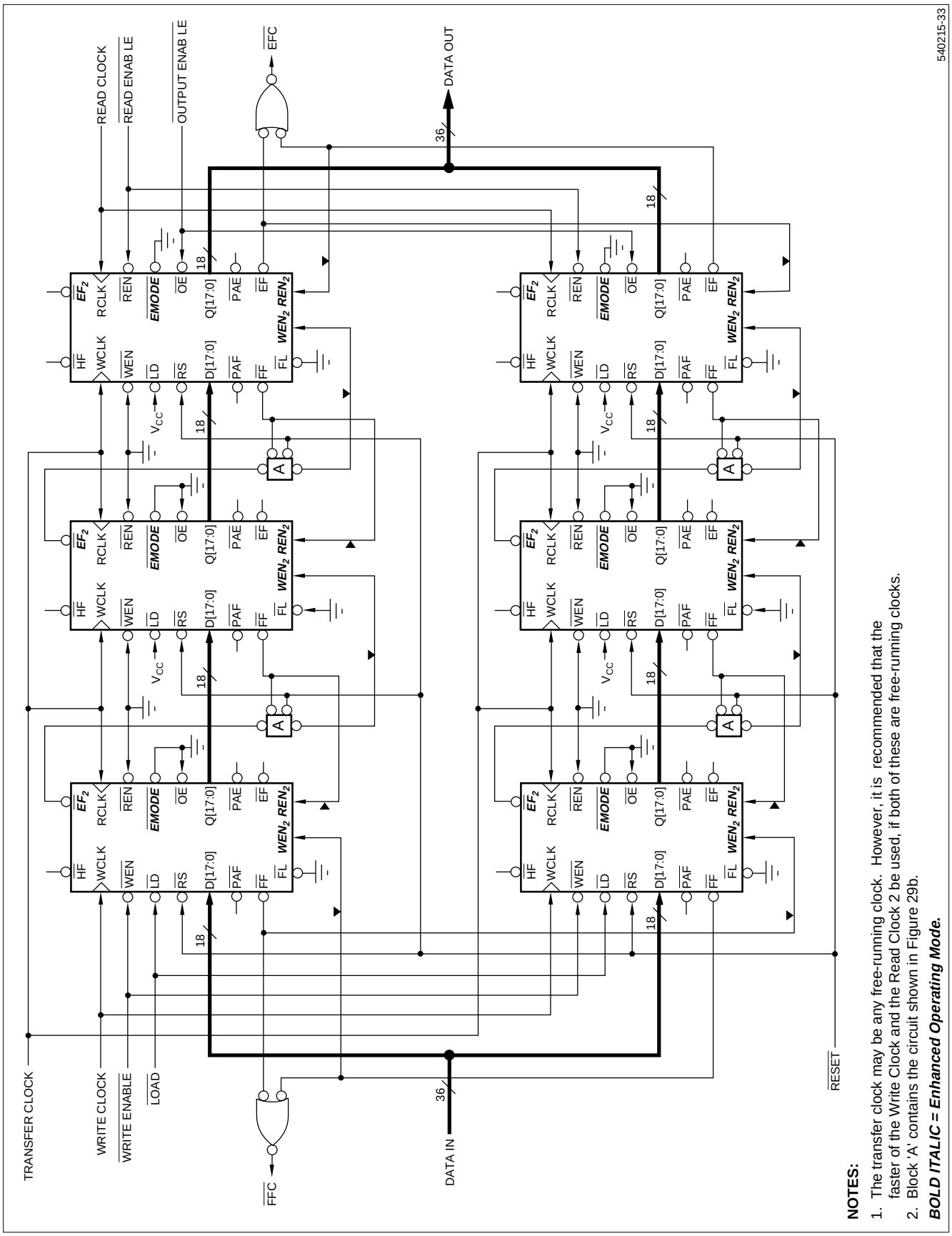
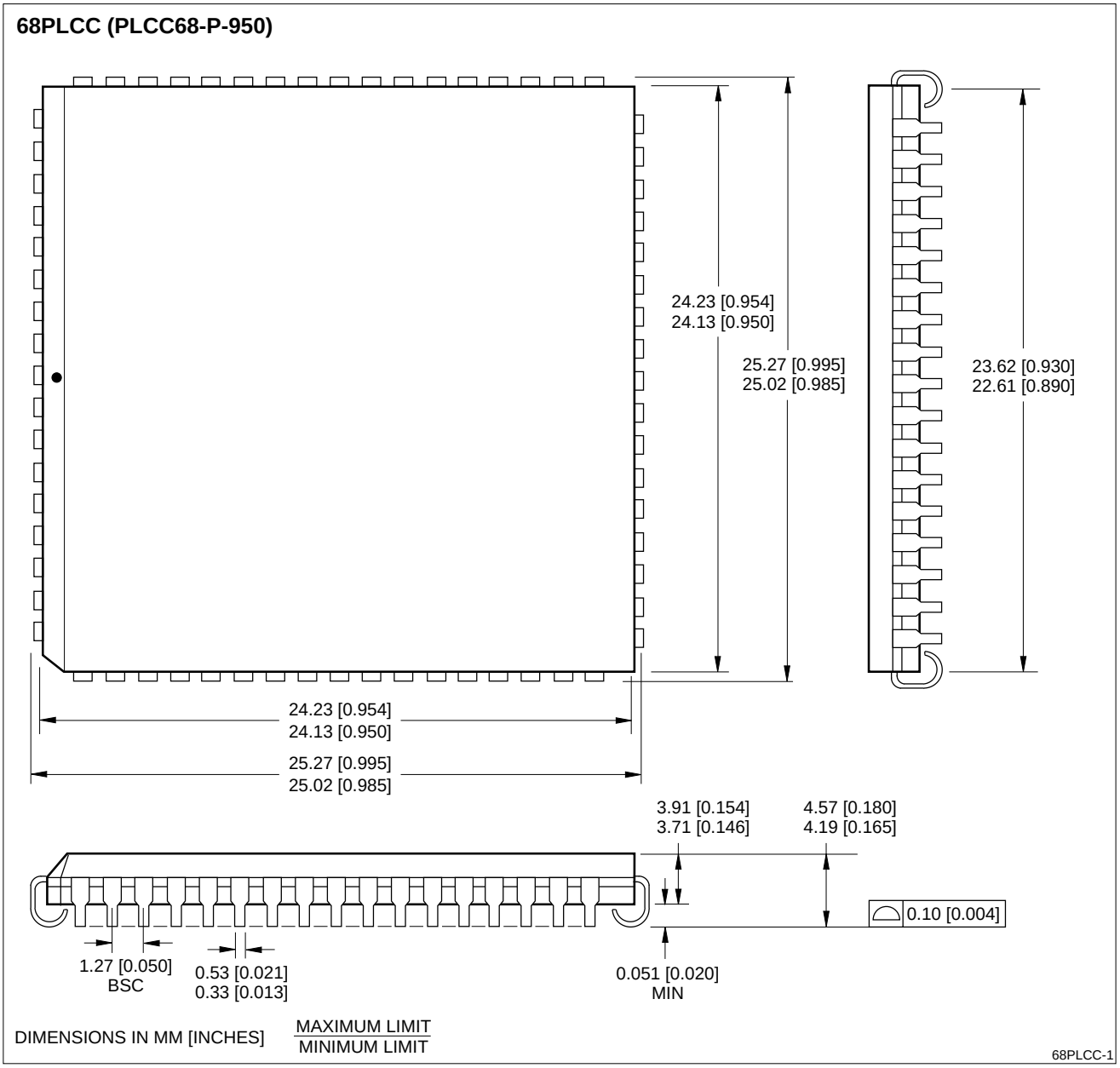


Figure 30. Interlocked Paralleling Used Together With Pipelined Depth-Cascading

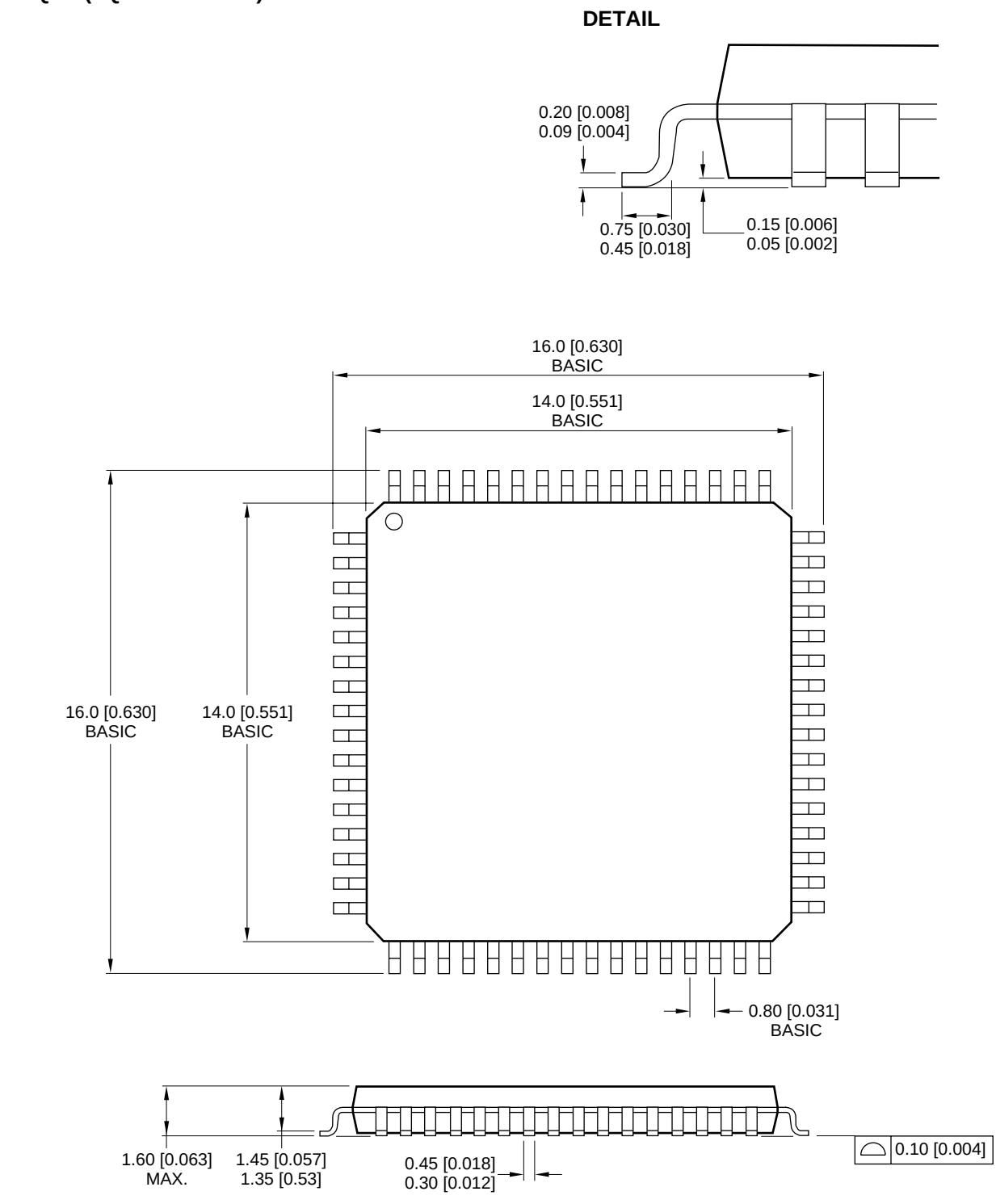
PACKAGE DIAGRAMS

68PLCC (PLCC68-P-950)



68-pin, 950-mil PLCC

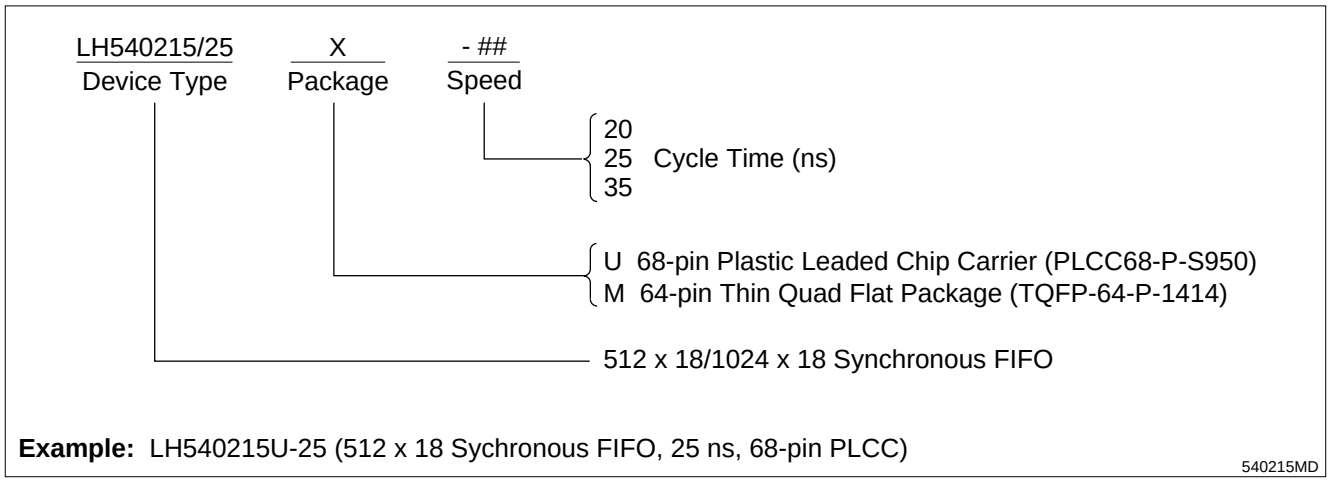
64TQFP (TQFP-64-P-1414)



64-pin TQFP

BOLD ITALIC = Enhanced Operating Mode

ORDERING INFORMATION



BOLD ITALIC = Enhanced Operating Mode