

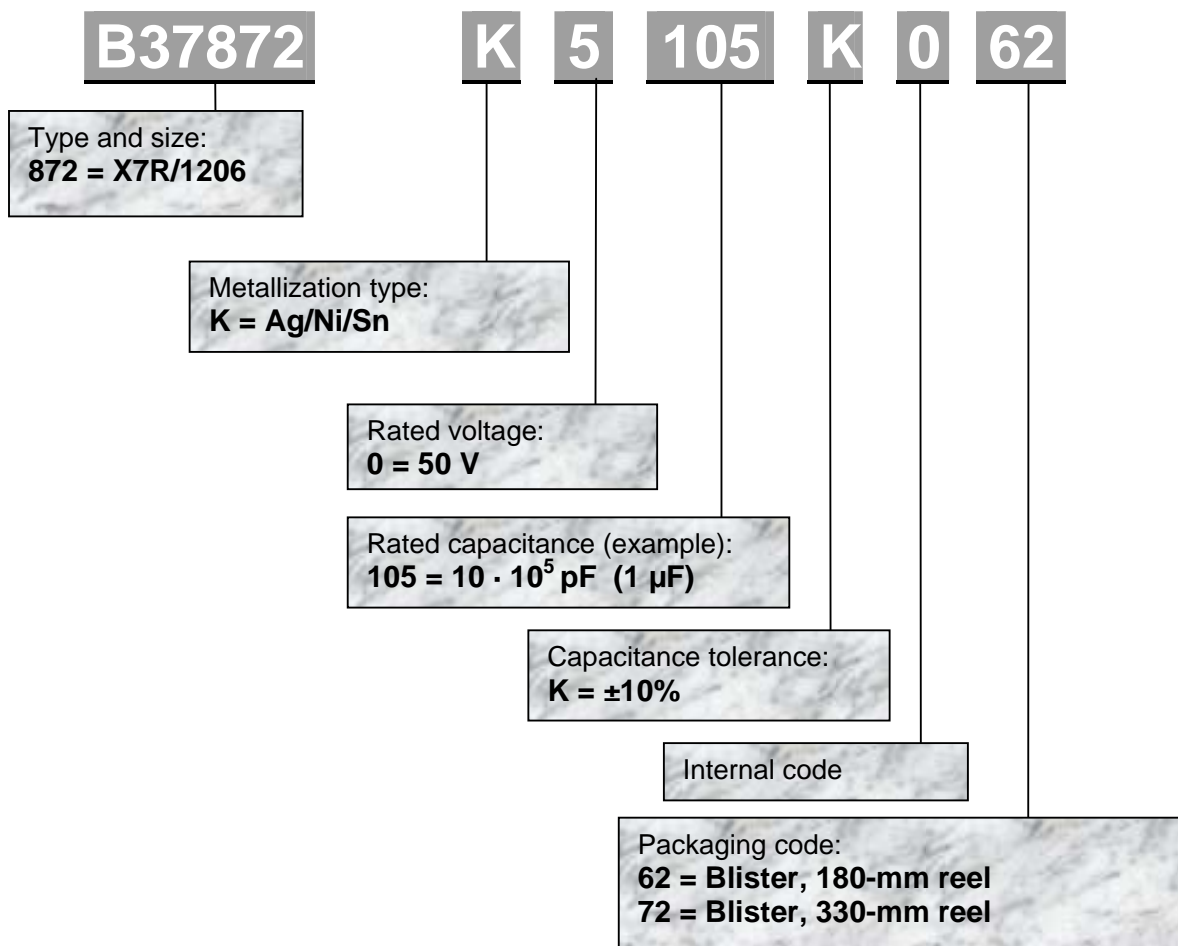


## Multilayer ceramic capacitor

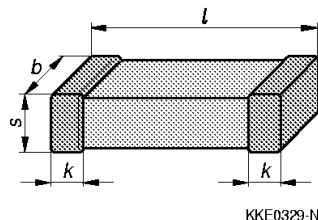
HighCV, X7R 1206 50 V

**Series/Type:** Chip  
**Ordering code:** B37872K5105K0\*\*  
Date: 25.10.2005  
Version: 1

### Ordering code



### Dimensional drawing



Size [inch / mm]	l [mm]	b [mm]	s [mm]	k [mm]
1206 / 3216	3.2 ±0.20	1.6 ±0.15	1.2 ±0.10	0.25 – 0.75

see also "Ordering codes and chip thickness", dimensions in accordance to CECC 32101-801



## Further information

Please see General Technical Information at [www.epcos.com/ceramic\\_capacitors](http://www.epcos.com/ceramic_capacitors) or the data book "Multilayer Ceramic Capacitors" for further information on:

- Soldering directions
- Taping and packing
- Surface mounting instructions
- Effects of mechanical stress

## Cautions and warnings

- Derating: A "state of the art" application design is essential to achieve failures rates at ppb level. Do not use designs based on 100% of specified rated values.
- AC applications may damage MLCC on a much lower level than DC voltage due to power dissipation losses.
- Mechanical stress - Please note EPCOS "General Technical Information", "Surface mounting instructions" and information about the effect of mechanical stress.
- ESD - EPCOS recommends the use of varistors.
- Further processing - care must be taken using moulding processes.
- Combined stresses - the total stress (e.g. DC voltage, AC ripple, pulses and temperature) has to be taken into account to estimate reliability of MLCC.

## Important notes

The following applies to all products named in this publication:

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