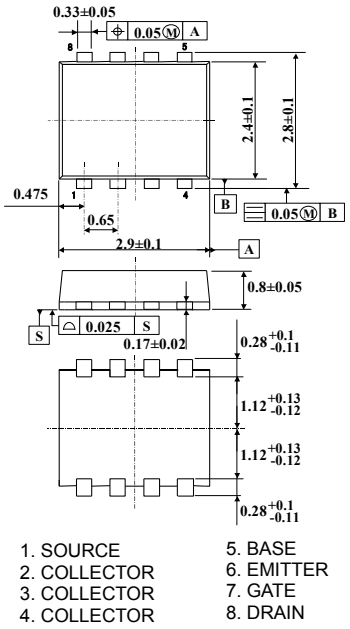
TOSHIBA Multi-Chip Transistor
Silicon NPN Epitaxial Type, Field Effect Transistor Silicon N Channel MOS Type

TPCP8H02

STROBE FLASH APPLICATIONS
HIGH-SPEED SWITCHING APPLICATIONS
DC-DC CONVERTER APPLICATIONS

- Multi-chip discrete device; built-in NPN transistor for main switch and N-ch MOS FET for drive
- High DC current gain: h_{FE} = 250 to 400 (I_C = 0.3 A) (NPN transistor)
- Low collector-emitter saturation voltage: $V_{CE\ (sat)}$ = 0.14 V (max) (NPN transistor)
- High-speed switching: t_f = 25 ns (typ.) (NPN transistor)



1. SOURCE
2. COLLECTOR
3. COLLECTOR
4. COLLECTOR
5. BASE
6. EMITTER
7. GATE
8. DRAIN

JEDEC	-
JEITA	-
TOSHIBA	2-3V1E

Absolute Maximum Ratings (Ta = 25°C)

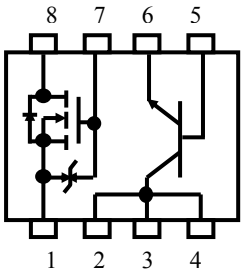
Transistor

Characteristics		Symbol	Rating	Unit
Collector-base voltage		V_{CBO}	50	V
Collector-emitter voltage		V_{CEX}	50	V
		V_{CEO}	30	
Emitter-base voltage		V_{EBO}	6	V
Collector current	DC (Note 1)	I_C	3.0	A
	Pulse (Note 1)	I_{CP}	5.0	
Base current		I_B	0.3	A
Collector power dissipation (NPN)		P_C (Note 2)	1.0	W
Junction temperature		T_j	150	°C

MOS FET

Characteristics		Symbol	Rating	Unit
Drain-Source Voltage		V_{DSS}	20	V
Gate-Source Voltage		V_{GSS}	±10	V
Drain Current	DC	I_D	100	mA
	Pulse	I_{DP}	200	
Channel Temperature		T_{ch}	150	°C

Circuit Configuration



Note 1: Ensure that the junction (channel) temperature does not exceed 150°C.

Note 2: Device mounted on a glass-epoxy board (FR-4,25.4 × 25.4 × 1.6 mm , Cu area: 645 mm^2)

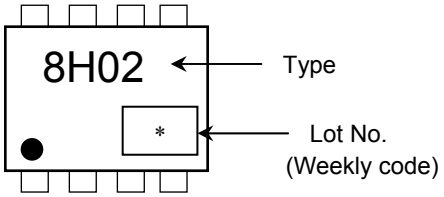
Note 3: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Please handle with caution.

Common Absolute Maximum Rating (Ta = 25°C)

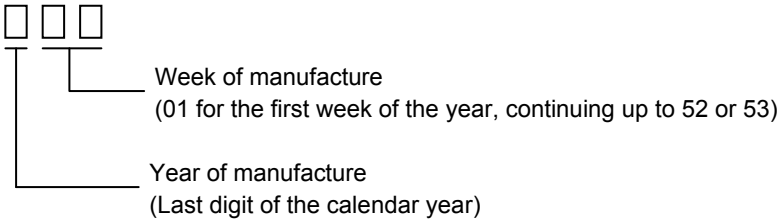
Characteristics	Symbol	Rating	Unit
Storage temperature range	T_{stg}	−55 to 150	°C

Marking (Note 4)



Note 4: The mark "●" on the lower left of the marking indicates Pin 1.

* Weekly code (three digits)

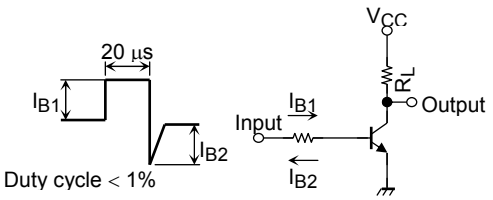


Electrical Characteristics (Ta = 25°C)

Transistor

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Collector cut-off current		I_{CBO}	V_{CB} = 50 V, I_E = 0	—	—	100	nA
Emitter cut-off current		I_{EBO}	V_{EB} = 6 V, I_C = 0	—	—	100	nA
Collector-emitter breakdown voltage		$V_{(BR)\ CEO}$	I_C = 10 mA, I_B = 0	30	—	—	V
DC current gain		h_{FE} (1)	V_{CE} = 2 V, I_C = 0.3 A	250	—	400	
		h_{FE} (2)	V_{CE} = 2 V, I_C = 1.0 A	120	—	—	
Collector-emitter saturation voltage		$V_{CE\ (sat)}$	I_C = 1.0 A, I_B = 33 mA	—	—	140	mV
Base-emitter saturation voltage		$V_{BE\ (sat)}$	I_C = 1.0 A, I_B = 33 mA	—	—	1.1	V
Collector output capacitance		C_{ob}	V_{CB} = 10V, I_E = 0, f=1MHz	—	18	—	pF
Switching time	Rise time	t_r	See Figure 1 circuit diagram.	—	40	—	ns
	Storage time	t_{stg}	V_{CC} ≒ 12 V, R_L = 12 Ω	—	320	—	
	Fall time	t_f	I_{B1} = -I_{B2} = 33 mA	—	25	—	

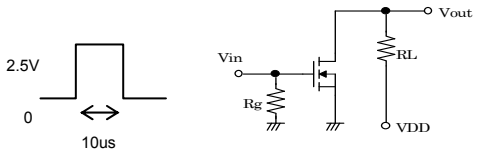
Figure 1 Switching Time Test Circuit & Timing Chart



MOS FET

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	—	±1	μA
Drain-source breakdown voltage		$V_{(BR)DSS}$	I_D = 0.1 mA, V_{GS} = 0	20	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = 20 V, V_{GS} = 0	—	—	1	μA
Gate threshold voltage		V_{th}	V_{DS} = 3V, I_D = 0.1mA	0.6	—	1.1	V
Forward transfer admittance		| Yfs |	V_{DS} = 3V, I_D = 10mA	40	—	—	mS
Drain-source ON-resistance		$R_{DS(ON)}$	I_D = 10mA , V_{GS} = 4V	—	1.5	3	Ω
			I_D = 10mA , V_{GS} = 2.5V	—	2.2	4	
			I_D = 1mA , V_{GS} = 1.5V	—	5.2	15	
Input capacitance		C_{iss}	V_{DS} = 3V, V_{GS} = 0, f=1MHz	—	9.3	—	pF
Reverse transfer capacitance		C_{rss}		—	4.5	—	
Output capacitance		C_{oss}		—	9.8	—	
Switching time	Turn-on time	t_{on}	See Figure 2 circuit diagram.	—	70	—	ns
	Turn-off time	t_{off}	V_{DD} ≒ 3V, R_L = 300 Ω V_{GS} = 0 to 2.5V	—	125	—	

Figure 2 Switching Time Test Circuit & Timing Chart



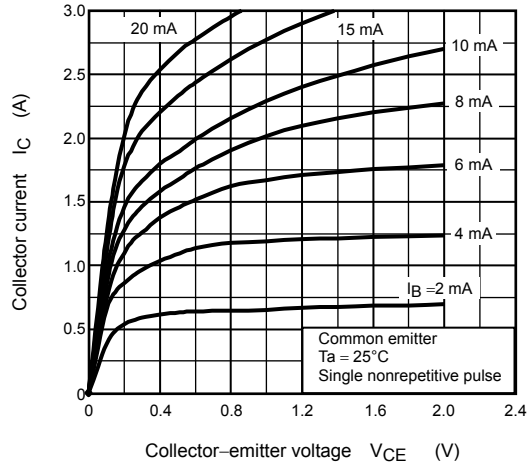
Gate Pulse Width 10 μ s, tr, tf<5ns
(Zout=50 Ω), Common Source, Ta=25°C
Duty Cycle<1%

Precautions

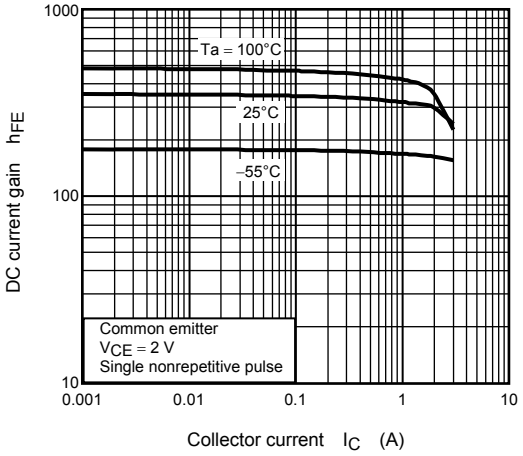
V_{th} can be expressed as the voltage between gate and source when the low operating current value is I_D=100 μA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than V_{th} and $V_{GS\ (off)}$ requires a lower voltage than V_{th}.
(The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$)
Please take this into consideration when using the device. The V_{GS} recommended voltage for turning on this product is 2.5 V or higher.

NPN

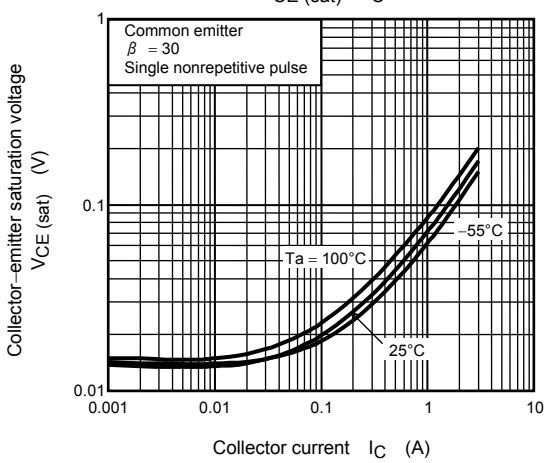
$I_C - V_{CE}$



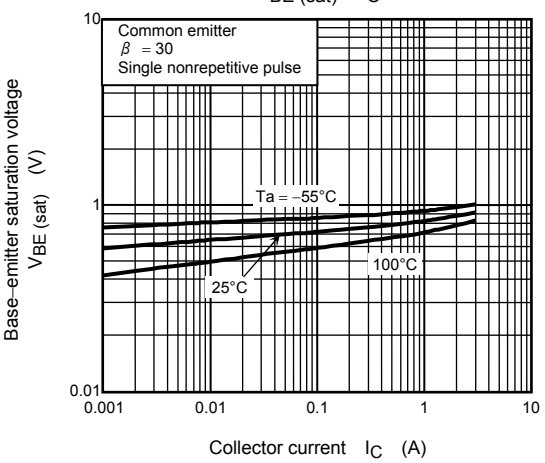
$h_{FE} - I_C$



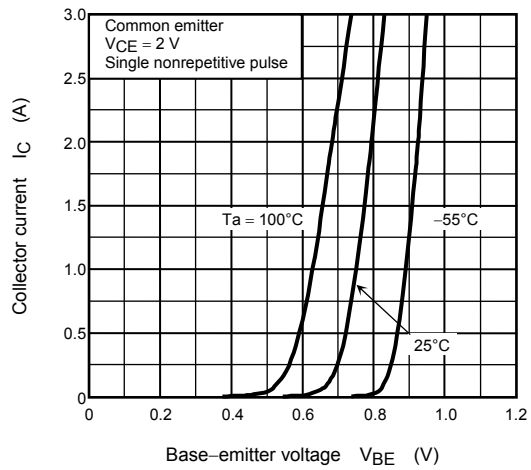
$V_{CE\ (sat)} - I_C$

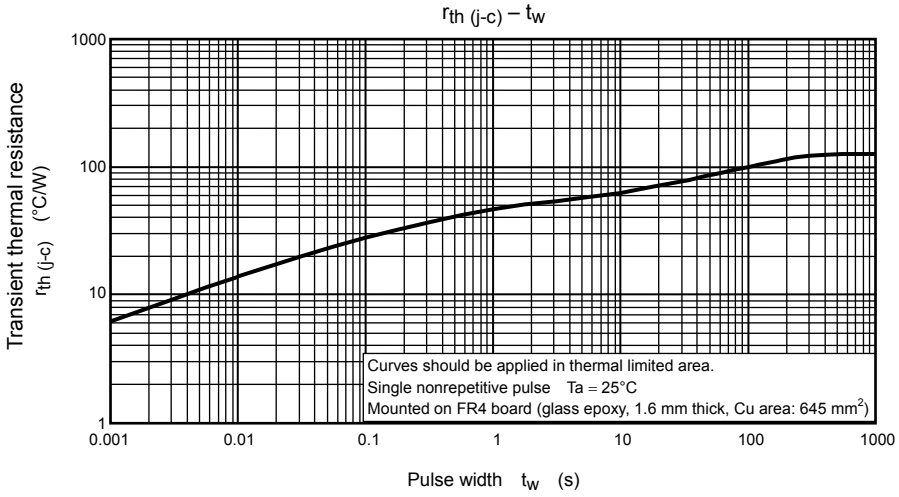


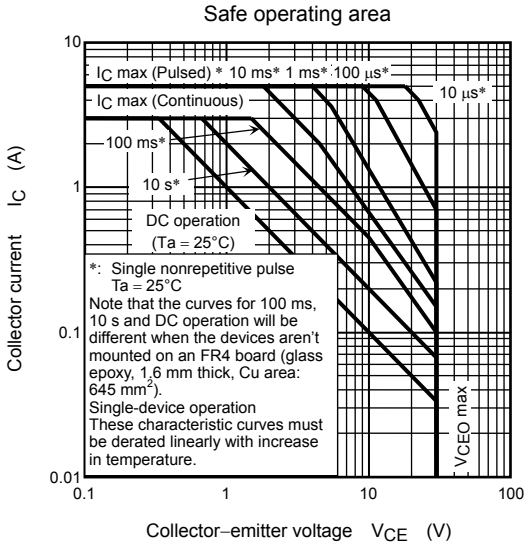
$V_{BE\ (sat)} - I_C$



$I_C - V_{BE}$

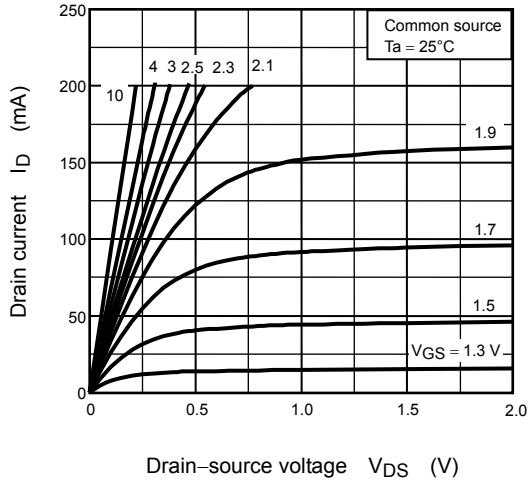



$r_{th\ (j\text{-}c)} - t_w$
Transient thermal resistance
$r_{th\ (j\text{-}c)}$ (°C/W)
1000
100
10
1
0.001
0.01
0.1
1
10
100
1000
Curves should be applied in thermal limited area.
Single nonrepetitive pulse Ta = 25°C
Mounted on FR4 board (glass epoxy, 1.6 mm thick, Cu area: 645 mm²)
Pulse width t_w (s)

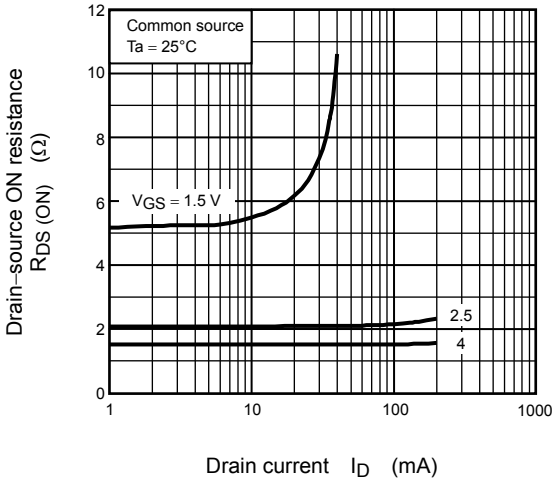

Safe operating area
I_C max (Pulsed) * 10 ms* 1 ms* 100 μs*
I_C max (Continuous)
10 μs*
100 ms*
10 s*
DC operation
(Ta = 25°C)
*: Single nonrepetitive pulse
Ta = 25°C
Note that the curves for 100 ms, 10 s and DC operation will be different when the devices aren't mounted on an FR4 board (glass epoxy, 1.6 mm thick, Cu area: 645 mm²).
Single-device operation
These characteristic curves must be derated linearly with increase in temperature.
V_{CEO} max
Collector current I_C (A)
10
1
0.1
0.01
0.1
1
10
100
Collector–emitter voltage V_{CE} (V)

Nch-MOS

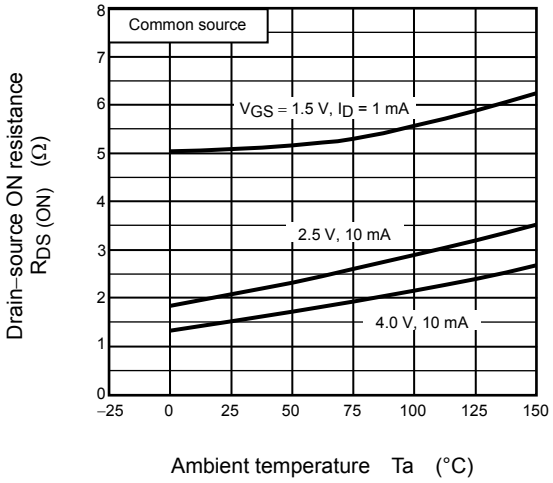
$I_D - V_{DS}$



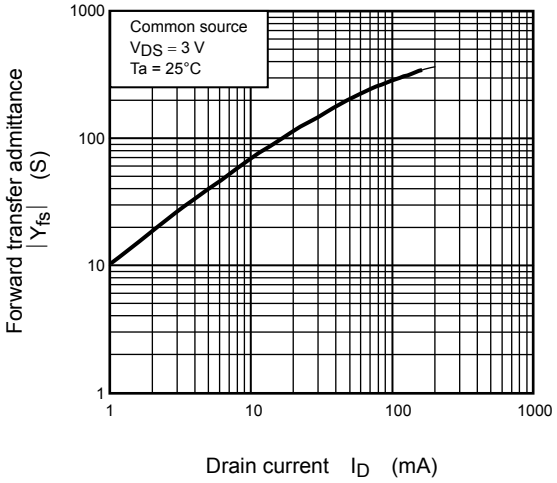
$R_{DS\ (ON)} - I_D$



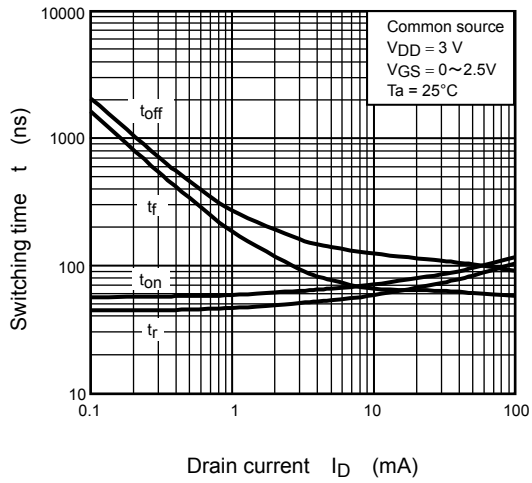
$R_{DS\ (ON)} - Ta$



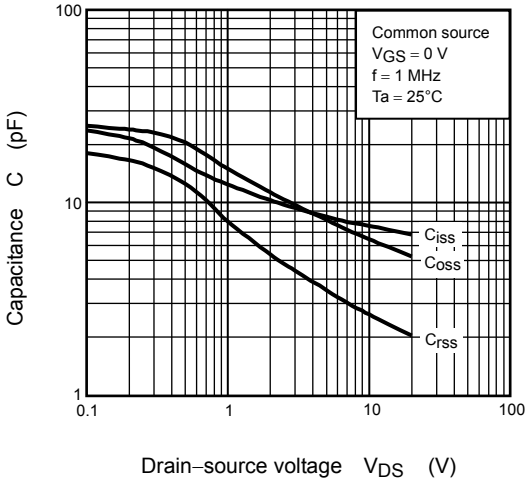
$|Y_{fs}| - I_D$



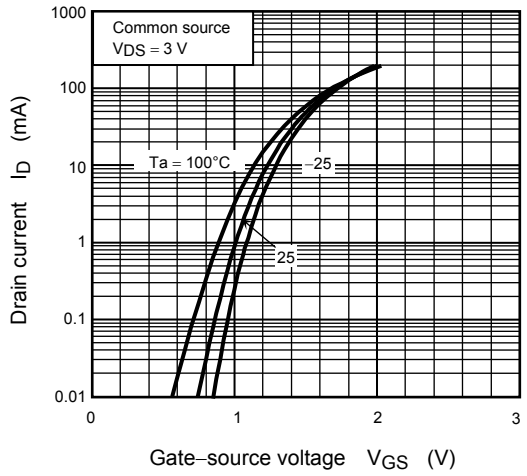
$t - I_D$



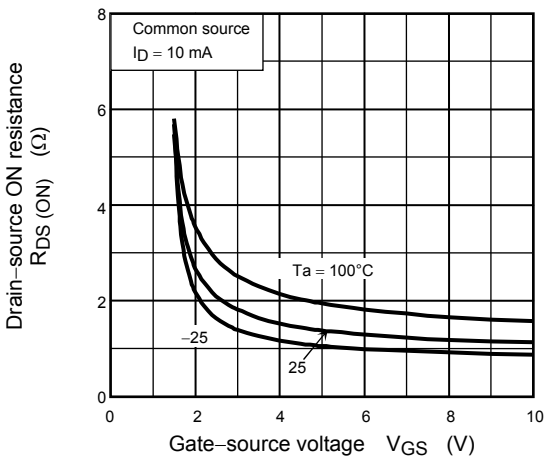
Capacitance $- V_{DS}$



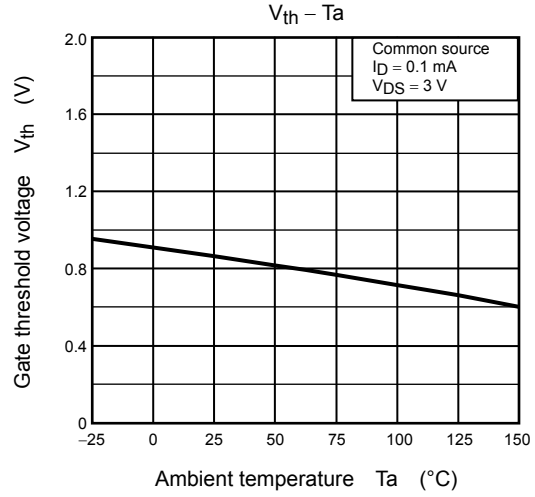
$I_D - V_{GS}$



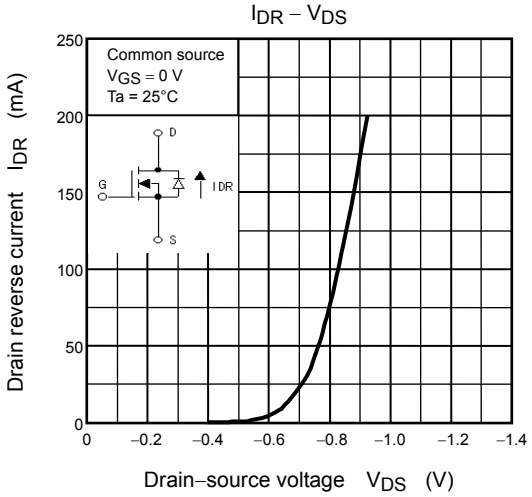
$R_{DS\ (ON)} - V_{GS}$



$V_{th} - Ta$



$I_{DR} - V_{DS}$



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