

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

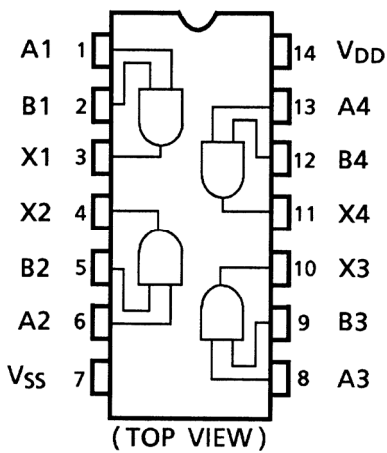
TC4081BP, TC4081BF, TC4081BFN

TC4081B Quad 2-Input AND Gate

TC4081B is positive logic AND gates with two inputs respectively.

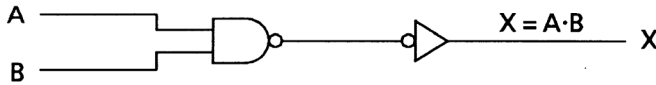
Since all the outputs of these gates are equipped with the buffer circuits of inverters, the input/output propagation characteristic has been improved and variation of propagation time caused by increase of load capacity is kept minimum.

Pin Assignment

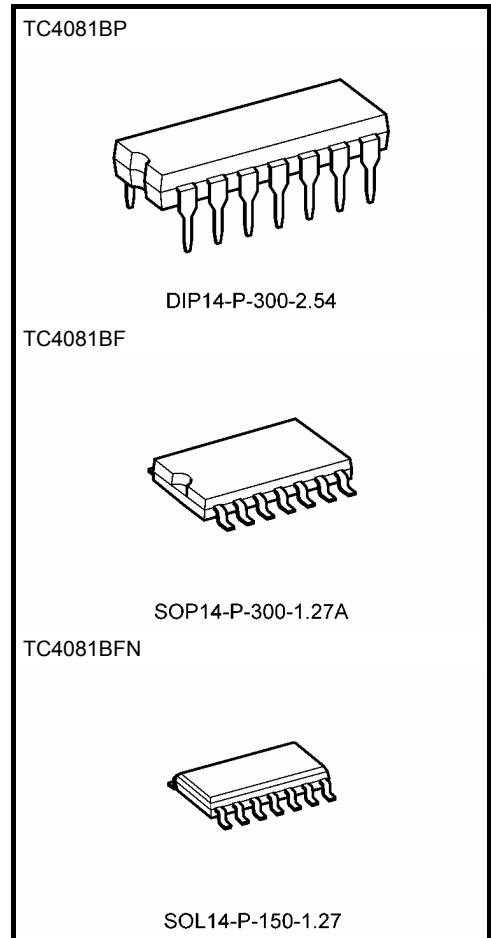


Logic Diagram

1/4 TC4081B



Note: xxxFN (JEDEC SOP) is not available in Japan.



Weight

DIP14-P-300-2.54	: 0.96 g (typ.)
SOP14-P-300-1.27A	: 0.18 g (typ.)
SOL14-P-150-1.27	: 0.12 g (typ.)

Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
DC supply voltage	V_{DD}	$V_{SS} - 0.5 \sim V_{SS} + 20$	V
Input voltage	V_{IN}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
Output voltage	V_{OUT}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
DC input current	I_{IN}	± 10	mA
Power dissipation	P_D	300 (DIP)/180 (SOIC)	mW
Operating temperature range	T_{ope}	-40~85	°C
Storage temperature range	T_{stg}	-65~150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges ($V_{SS} = 0$ V) (Note)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
DC supply voltage	V_{DD}	—	3	—	18	V
Input voltage	V_{IN}	—	0	—	V_{DD}	V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{DD} or V_{SS} .

Static Electrical Characteristics (V_{SS} = 0 V)

Characteristics	Sym- bol	Test Condition	V _{DD} (V)	-40°C		25°C			85°C		Unit	
				Min	Max	Min	Typ.	Max	Min	Max		
High-level output voltage	V _{OH}	I _{OUT} < 1 μA V _{IN} = V _{SS} , V _{DD}	5	4.95	—	4.95	5.00	—	4.95	—	V	
			10	9.95	—	9.95	10.00	—	9.95	—		
			15	14.95	—	14.95	15.00	—	14.95	—		
Low-level output voltage	V _{OL}	I _{OUT} < 1 μA V _{IN} = V _{SS} , V _{DD}	5	—	0.05	—	0.00	0.05	—	0.05	V	
			10	—	0.05	—	0.00	0.05	—	0.05		
			15	—	0.05	—	0.00	0.05	—	0.05		
Output high current	I _{OH}	V _{OH} = 4.6 V V _{OH} = 2.5 V V _{OH} = 9.5 V V _{OH} = 13.5 V V _{IN} = V _{DD}	5	-0.61	—	-0.51	-1.0	—	-0.42	—	mA	
			5	-2.50	—	-2.10	-4.0	—	-1.70	—		
			10	-1.50	—	-1.30	-2.2	—	-1.10	—		
			15	-4.00	—	-3.40	-9.0	—	-2.80	—		
Output low current	I _{OL}	V _{OL} = 0.4 V V _{OL} = 0.5 V V _{OL} = 1.5 V V _{IN} = V _{SS} , V _{DD}	5	0.61	—	0.51	1.2	—	0.42	—	mA	
			10	1.50	—	1.30	3.2	—	1.10	—		
			15	4.00	—	3.40	12.0	—	2.80	—		
			—	—	—	—	—	—	—	—		
Input high voltage	V _{IH}	V _{OUT} = 0.5 V, 4.5 V V _{OUT} = 1.0 V, 9.0 V V _{OUT} = 1.5 V, 13.5 V I _{OUT} < 1 μA	5	3.5	—	3.5	2.75	—	3.5	—	V	
			10	7.0	—	7.0	5.50	—	7.0	—		
			15	11.0	—	11.0	8.25	—	11.0	—		
			—	—	—	—	—	—	—	—		
Input low voltage	V _{IL}	V _{OUT} = 0.5 V, 4.5 V V _{OUT} = 1.0 V, 9.0 V V _{OUT} = 1.5 V, 13.5 V I _{OUT} < 1 μA	5	—	1.5	—	2.25	1.5	—	1.5	V	
			10	—	3.0	—	4.50	3.0	—	3.0		
			15	—	4.0	—	6.75	4.0	—	4.0		
			—	—	—	—	—	—	—	—		
Input current	"H" level	I _{IH}	V _{IH} = 18 V	18	—	0.1	—	10 ⁻⁵	0.1	—	1.0	μA
	"L" level	I _{IL}	V _{IL} = 0 V	18	—	-0.1	—	-10 ⁻⁵	-0.1	—	-1.0	
Quiescent supply current	I _{DD}	V _{IN} = V _{SS} , V _{DD} (Note)	5	—	0.25	—	0.001	0.25	—	7.5	μA	
			10	—	0.50	—	0.001	0.50	—	15.0		
			15	—	1.00	—	0.002	1.00	—	30.0		

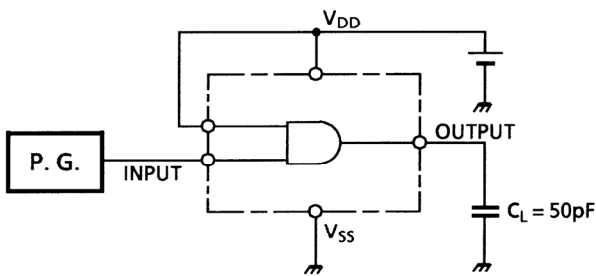
Note: All valid input combinations.

Dynamic Electrical Characteristics (Ta = 25°C, VSS = 0 V, CL = 50 pF)

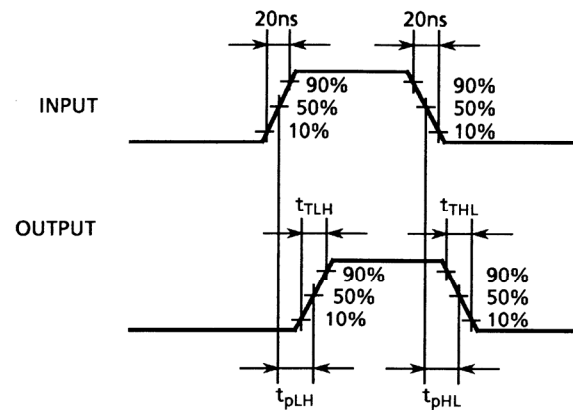
Characteristics	Symbol	Test Condition	VDD (V)	Min	Typ.	Max	Unit
			5	10	15	—	—
Output transition time (low to high)	t _{TLH}	—	5	—	70	200	ns
			10	—	35	100	
			15	—	30	80	
Output transition time (high to low)	t _{THL}	—	5	—	70	200	ns
			10	—	35	100	
			15	—	30	80	
Propagation delay time	t _{pLH}	—	5	—	65	200	ns
			10	—	30	100	
			15	—	25	80	
Propagation delay time	t _{pHL}	—	5	—	65	200	ns
			10	—	30	100	
			15	—	25	80	
Input capacitance	C _{IN}	—	—	5	7.5	pF	

Circuit and Waveform for Measurement of Dynamic Characteristics

Circuit



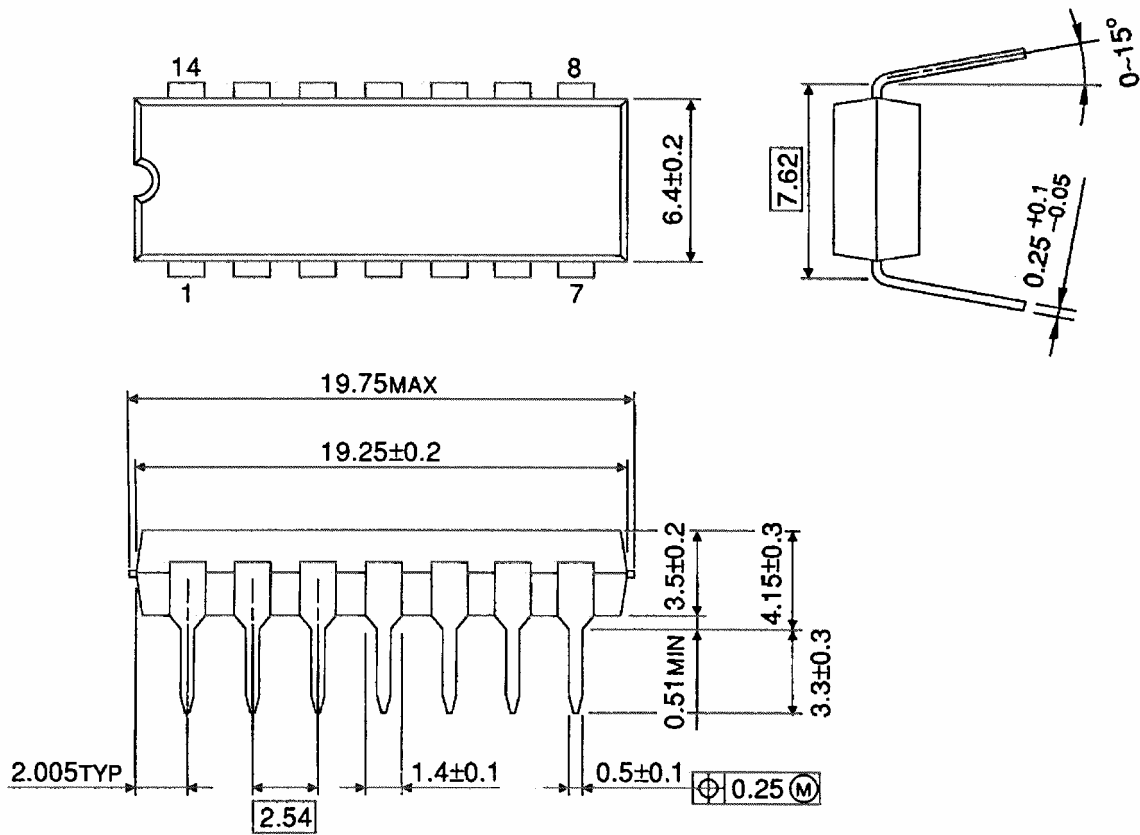
Waveform



Package Dimensions

DIP14-P-300-2.54

Unit : mm

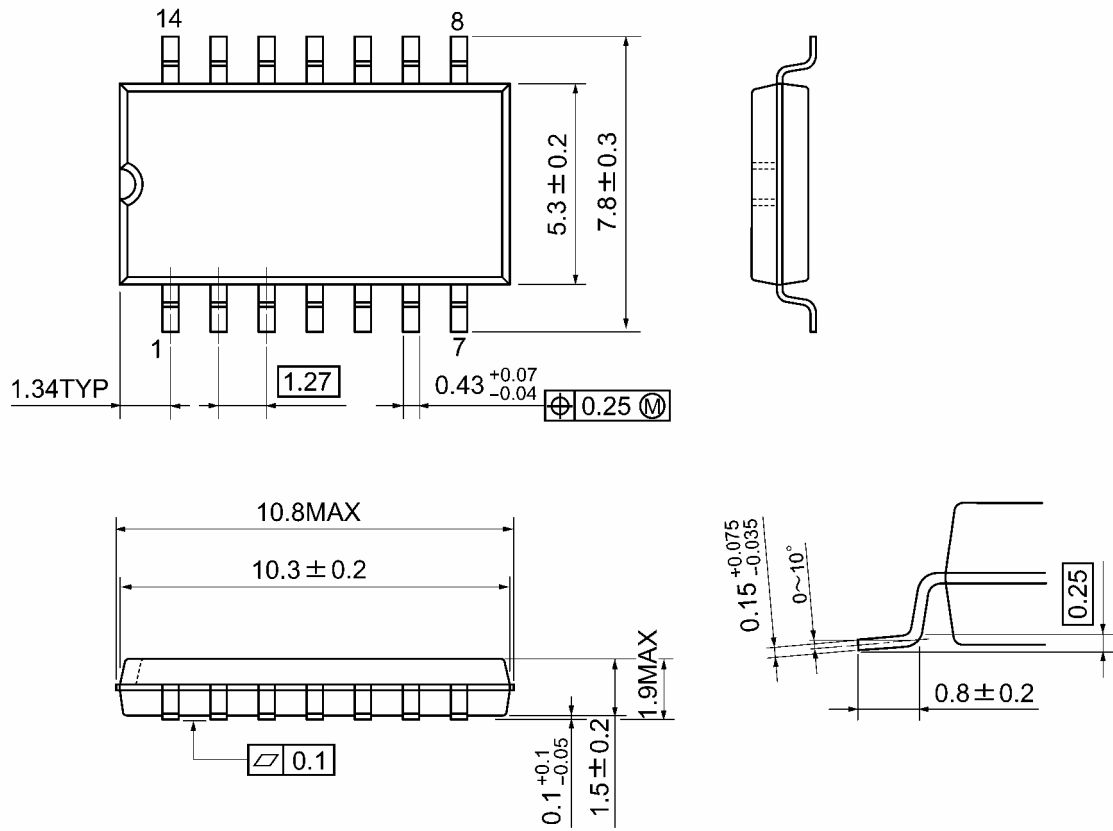


Weight: 0.96 g (typ.)

Package Dimensions

SOP14-P-300-1.27A

Unit: mm

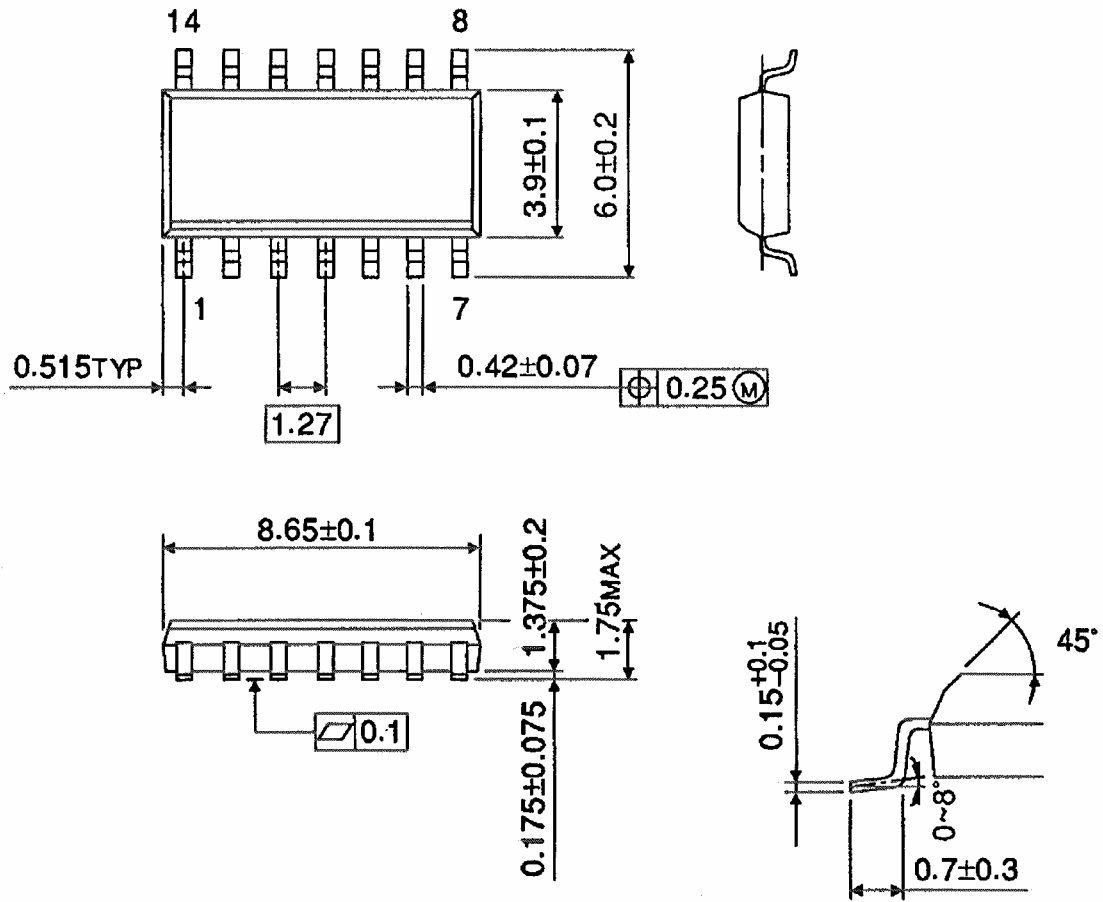


Weight: 0.18 g (typ.)

Package Dimensions (Note)

SOL14-P-150-1.27

Unit : mm



Note: This package is not available in Japan.

Weight: 0.12 g (typ.)

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20070701-EN GENERAL

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