

TC74VHC4040F, TC74VHC4040FN, TC74VHC4040FT, TC74VHC4040FK

12-Stage Ripple Carry Binary Counter

The TC74VHC4040 is an advanced high speed CMOS 12-STAGE BINARY COUNTER/DIVIDER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

Setting CLR to high resets the counter to low.

A negative transition on the \overline{CK} input brings one increment into the counter.

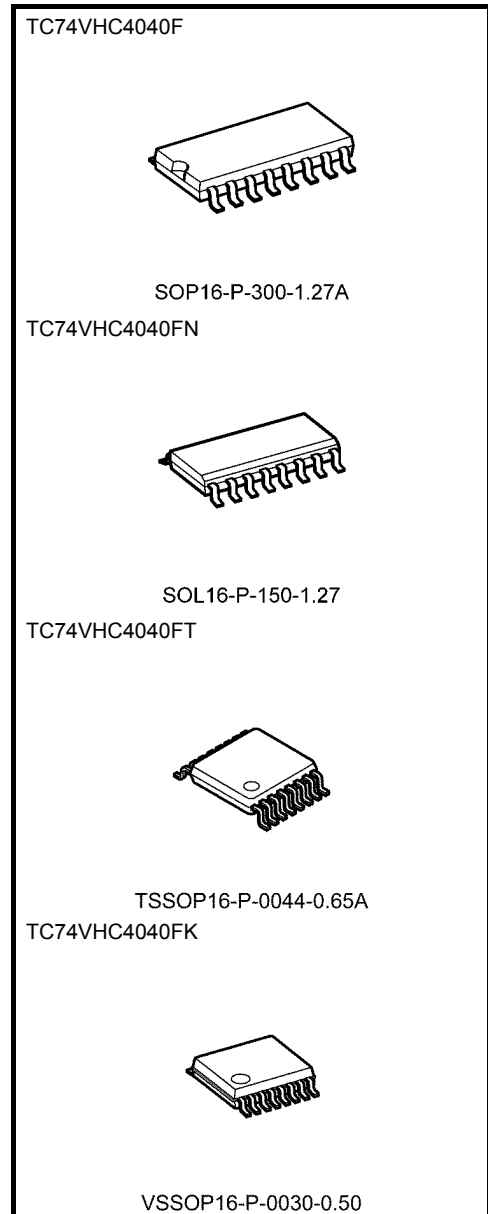
This counter provides all divided output stages, and at Q12, a 1/4096 divided frequency will be output.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

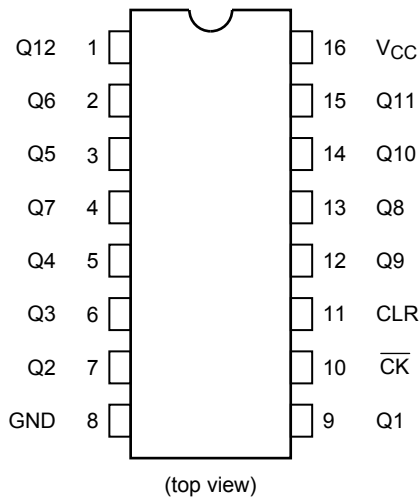
- High speed: $f_{max} = 210$ MHz (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 4$ μ A (max) at $T_a = 25^\circ$ C
- High noise immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC} (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: $V_{CC(opr)} = 2$ V to 5.5 V
- Low noise: $V_{OLP} = 1.5$ V (max)
- Pin and function compatible with 74HC4040

Note: xxxFN (JEDEC SOP) is not available in Japan.

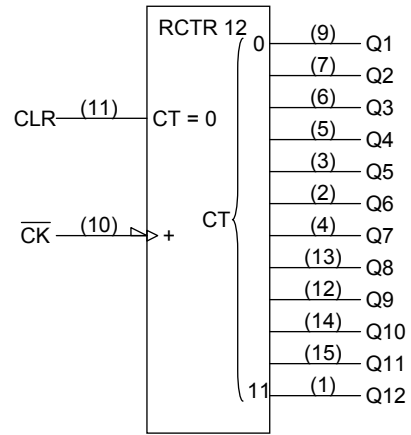


Weight	
SOP16-P-300-1.27A	: 0.18 g (typ.)
SOL16-P-150-1.27	: 0.13 g (typ.)
TSSOP16-P-0044-0.65A	: 0.06 g (typ.)
VSSOP16-P-0030-0.50	: 0.02 g (typ.)

Pin Assignment



IEC Logic Symbol

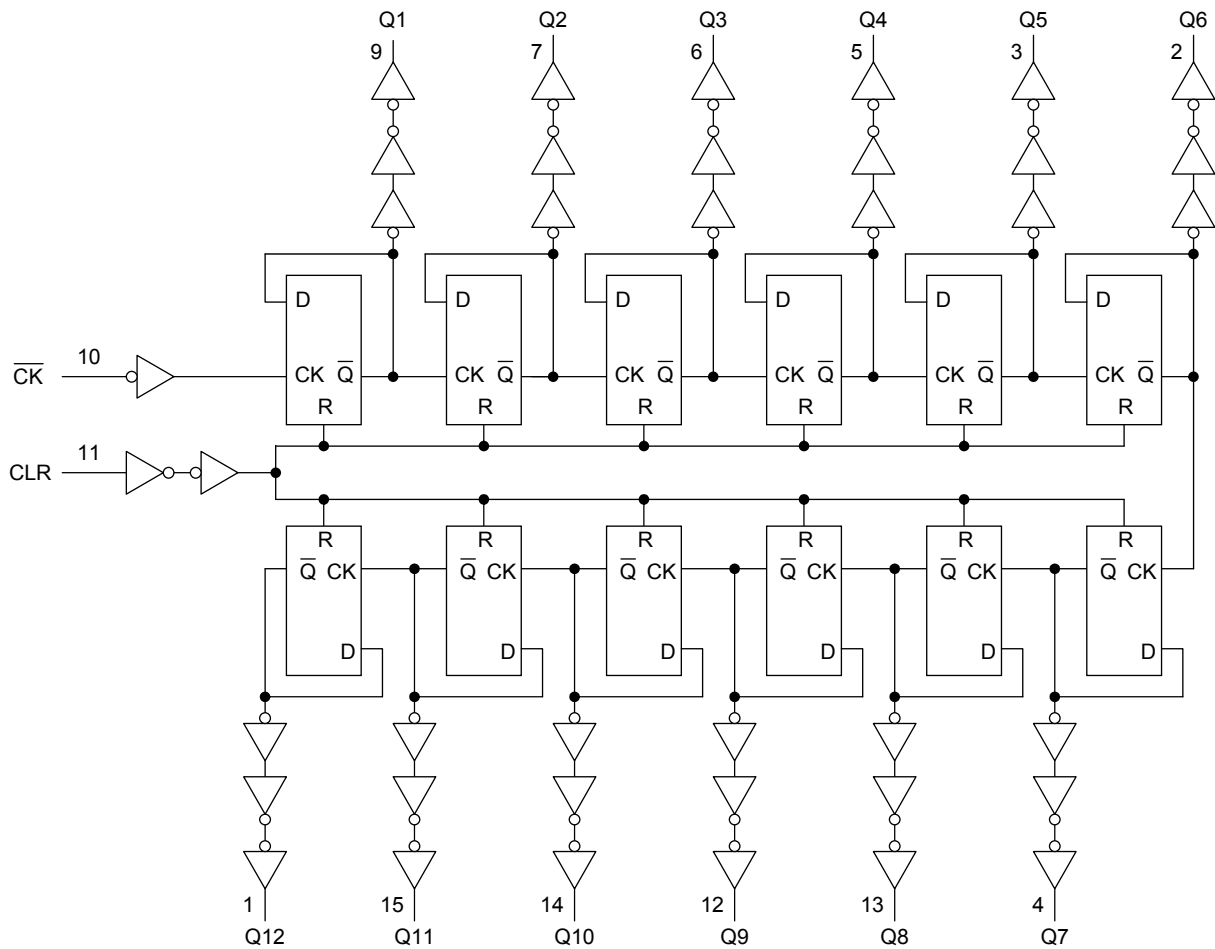


Truth Table

\overline{CK}	CLR	Output State
X	H	All Outputs = "L"
\uparrow	L	No Change
\downarrow	L	Advance to Next State

X: Don't care

System Diagram



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to 7.0	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /ground current	I_{CC}	± 100	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100 ($V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ($V_{CC} = 5 \pm 0.5$ V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition	$T_a = 25^\circ\text{C}$			$T_a = -40$ to 85°C		Unit		
			V_{CC} (V)	Min	Typ.	Max	Min		Max	
High-level input voltage	V_{IH}	—	2.0 3.0 to 5.5	1.50 $V_{CC} \times 0.7$	— —	— —	1.50 $V_{CC} \times 0.7$	— —	V	
Low-level input voltage	V_{IL}	—	2.0 3.0 to 5.5	— —	— —	0.50 $V_{CC} \times 0.3$	— —	0.50 $V_{CC} \times 0.3$	V	
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50 \mu\text{A}$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
			$I_{OH} = -4 \text{ mA}$	3.0 4.5	2.58 3.94	— —	— —	2.48 3.80	— —	
			$I_{OH} = -8 \text{ mA}$	3.0 4.5	— —	— —	— —	— —	— —	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50 \mu\text{A}$	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			$I_{OL} = 4 \text{ mA}$	3.0 4.5	— —	— —	0.36 0.36	— —	0.44 0.44	
			$I_{OL} = 8 \text{ mA}$	3.0 4.5	— —	— —	0.36 0.36	— —	0.44 0.44	
Input leakage current	I_{IN}	$V_{IN} = 5.5 \text{ V}$ or GND	0 to 5.5	—	—	± 0.1	—	± 1.0	μA	
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	—	40.0	μA	

Timing Requirements (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C	Unit
			V _{CC} (V)	Typ.	Limit	
Minimum pulse width ($\overline{\text{CK}}$)	t_w (L)	—	3.3 ± 0.3	—	5.0	ns
	t_w (H)		5.0 ± 0.5	—	5.0	
Minimum pulse width (CLR)	t_w (H)	—	3.3 ± 0.3	—	5.0	ns
			5.0 ± 0.5	—	5.0	
Minimum removal time	t_{rem}	—	3.3 ± 0.3	—	5.0	ns
			5.0 ± 0.5	—	5.0	

AC Characteristics (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit		
			V _{CC} (V)	C _L (pF)	Min	Typ.	Max		Min	Max
Propagation delay time ($\overline{\text{CK}} - \text{Q1}$)	t_{pLH}	—	3.3 ± 0.3	15	—	7.5	11.9	1.0	14.0	ns
				50	—	10.0	15.4	1.0	17.5	
	5.0 ± 0.5	15	—	4.8	7.3	1.0	8.5			
		50	—	6.3	9.3	1.0	10.5			
Propagation delay time ($\text{Q}_n - \text{Q}_{n+1}$)	Δt_{pd}	—	3.3 ± 0.3	50	—	2.4	4.4	—	5.0	ns
				5.0 ± 0.5	50	—	1.6	3.1	—	
Propagation delay time (CLR-Q)	t_{pHL}	—	3.3 ± 0.3	15	—	8.3	12.8	1.0	15.0	ns
				50	—	10.8	16.3	1.0	18.5	
			5.0 ± 0.5	15	—	5.6	8.6	1.0	10.0	
				50	—	7.1	10.6	1.0	12.0	
Maximum clock frequency	f_{max}	—	3.3 ± 0.3	15	75	140	—	75	—	MHz
				50	55	80	—	50	—	
			5.0 ± 0.5	15	150	210	—	125	—	
				50	95	125	—	80	—	
Input capacitance	C _{IN}	—	—	4	10	—	10	pF		
Power dissipation capacitance	C _{PD}	(Note)	—	21	—	—	—	pF		

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

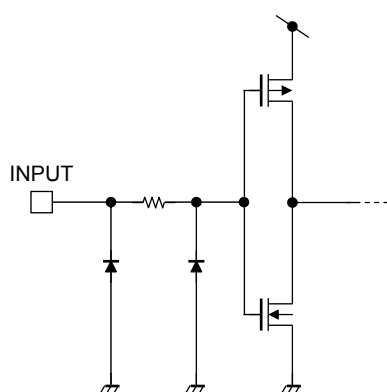
Average operating current can be obtained by the equation:

$$I_{\text{CC (opr)}} = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}}$$

Noise Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C		Unit
			V _{CC} (V)	Typ. Limit	
Quiet output maximum dynamic V _{OL}	V _{OLP}	C _L = 50 pF	5.0	1.2 1.5	V
Quiet output minimum dynamic V _{OL}	V _{OLV}	C _L = 50 pF	5.0	-1.2 -1.5	V
Minimum high level dynamic input voltage	V _{IHD}	C _L = 50 pF	5.0	— 3.5	V
Maximum low level dynamic input voltage	V _{ILD}	C _L = 50 pF	5.0	— 1.5	V

Input Equivalent Circuit



Package Dimensions

SOP16-P-300-1.27A

Unit: mm

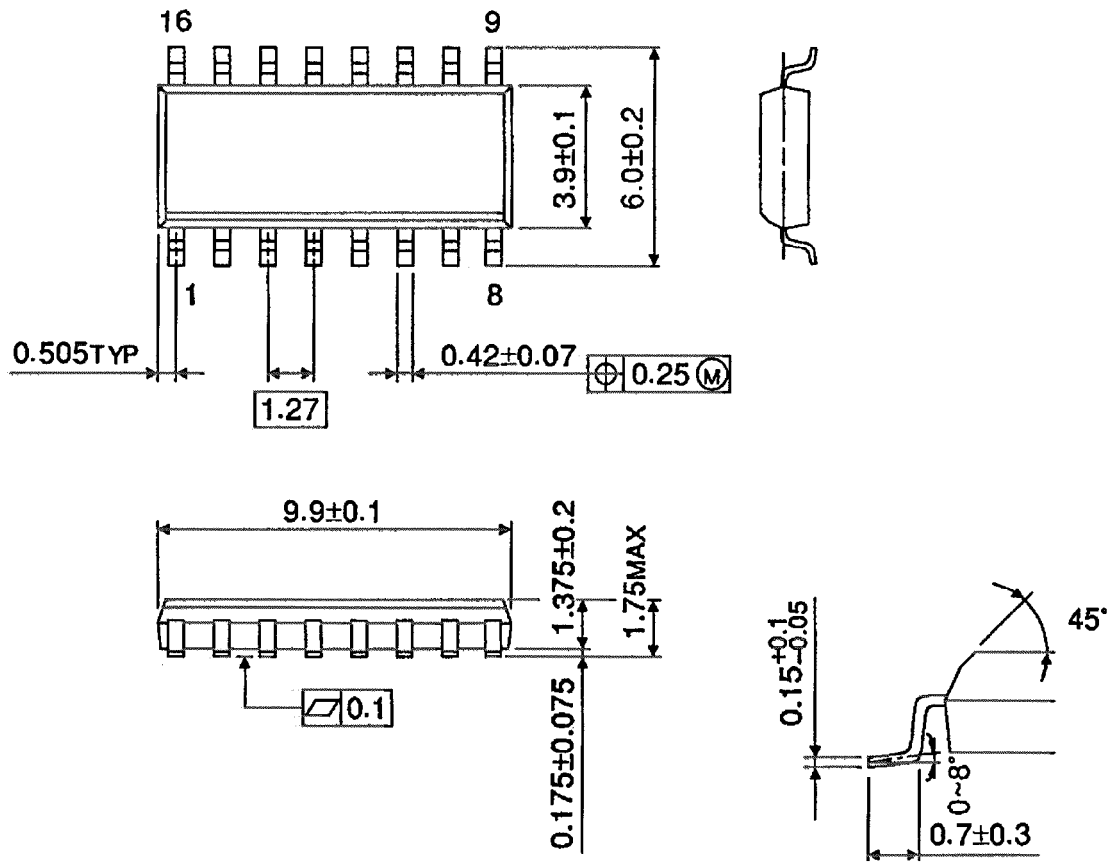


Weight: 0.18 g (typ.)

Package Dimensions (Note)

SOL16-P-150-1.27

Unit : mm



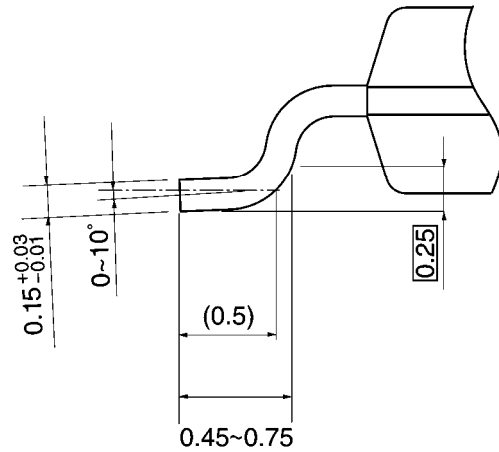
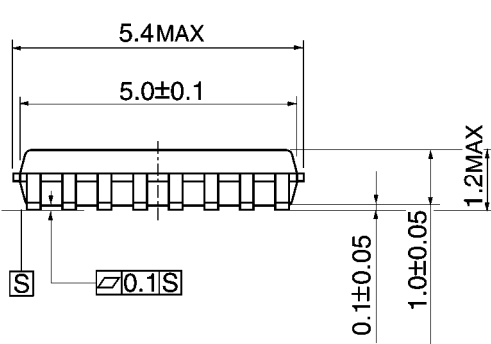
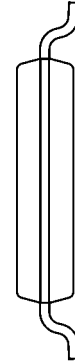
Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

Package Dimensions

TSSOP16-P-0044-0.65A

Unit: mm

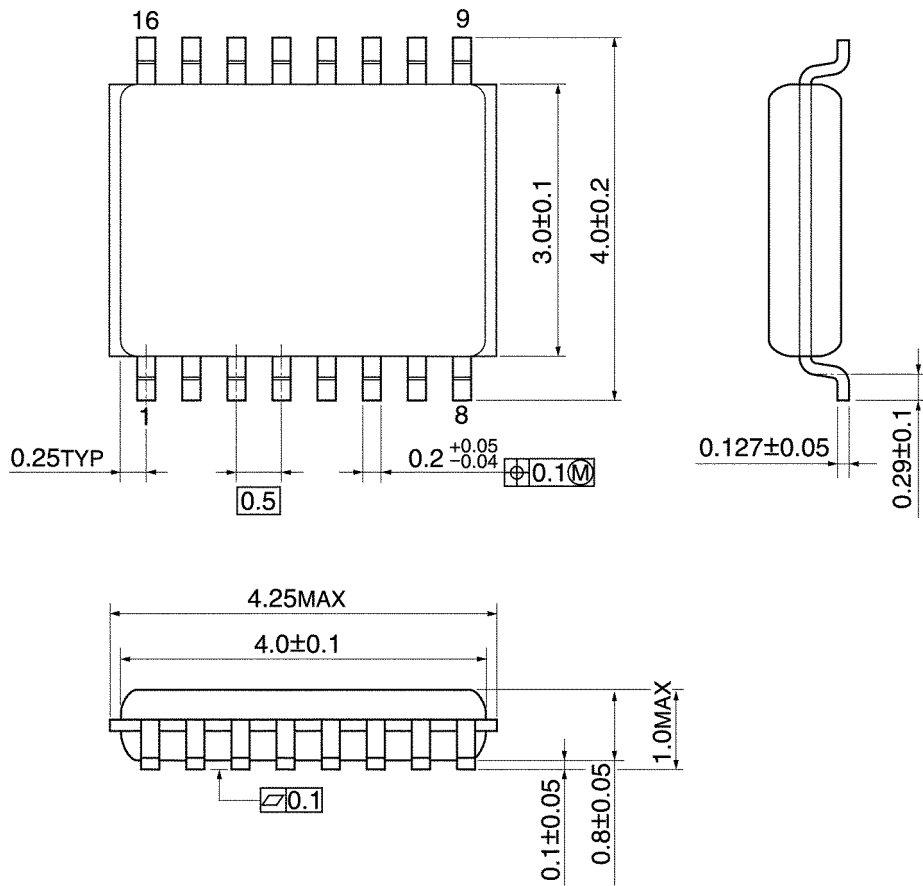


Weight: 0.06 g (typ.)

Package Dimensions

VSSOP16-P-0030-0.50

Unit: mm



Weight: 0.02 g (typ.)

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