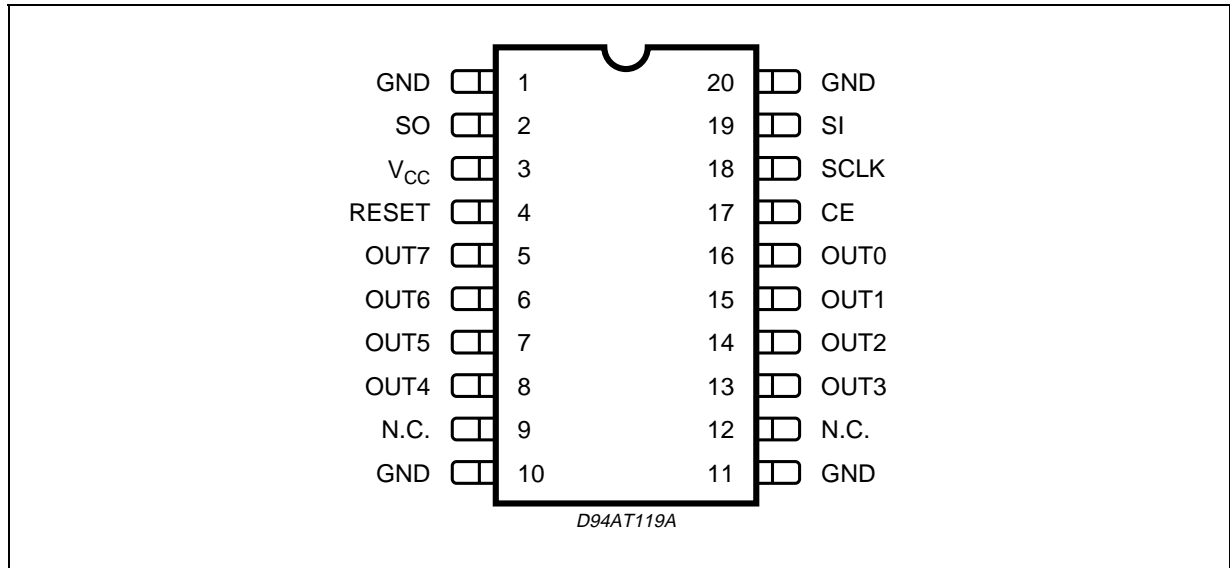


L9822N

PIN CONNECTIONS (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
V_{CC}	DC Logic Supply	- 0.7	7	V
V_O	Output Voltage	- 0.7	40	V
I_I	Input Transient Current (CE, SI, SCLK, RESET, SO) : Duration Time $t = 1s$, $V_I < 0$ $V_I > V_{CC}$	- 25	+ 25	mA mA
T_j, T_{stg}	Junction and Storage Temperature Range	- 40	150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j-case}$	Thermal Resistance Junction-Case	Max. 1.5	°C/W
$R_{th\ j-amb}$	Thermal Resistance Junction-Ambient	Max. 60	°C/W

PIN DESCRIPTION

V_{CC}

Logic supply voltage - nominally 5V

GROUND

Device Ground. This ground applies for the logic circuits as well as the power output stages.

RESET

Asynchronous reset for the output stages, the parallel latch and the shift register inside the L9822NSP. This pin is active low and it must not be left floating. A power on clear function may be implemented connecting this pin to V_{CC} with an external resistor and to ground with an external capacitor.

CE

Chip Enable. Data is transferred from the shift registers to the outputs on the rising edge of this signal. The falling edge of this signal sets the shift register with the output voltage sense bits coming from the output stages. The output driver for the SO pin is enabled when this pin is low.

SO

Serial Output. This pin is the serial output from the shift register and it is tri-stated when CE is high. A high for a data bit on this pin indicates that the par-

ticular output is high. A low on this pin for a data bit indicates that the output is low.

Comparing the serial output bits with the previous serial input bits the external microcontroller implements the diagnostic data supplied by the L9822.

SI

Serial Input. This pin is the serial data input. A high on this pin will program a particular output to be OFF, while a low will turn it ON.

SCLK

Serial Clock. This pin clocks the shift register. New SO data will appear on every rising edge of this pin and new SI data will be latched on every SCLK's falling edge into the shift register.

OUTPUTS 00-07

Power output pins. The input and output bits corresponding to 07 are sent and received first via the SPI bus and 00 is the last.

The outputs are provided with current limiting and voltage sense functions for fault indication and protection. The nominal load current for these outputs is 500mA. The outputs also have on board clamps set at about 36V for recirculation of inductive load current.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 5%, T_j = -40 to 125°C ; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{OC}	Output Clamping Volt.	I _O = 0.5A, Output Programmed OFF	30	35	40	V
E _{OC}	Out. Clamping Energy	I _O = 0.5A, When ON	20			mJ
I _{OFF}	Out. Leakage Current	V _O = 24V, Output Progr. OFF			1	mA
R _{DSon}	On Resistance	Output Progr. ON I _O = 0.5A I _O = 0.75A I _O = 1A With Fault Reset Disabled		0.53 0.53 0.53	1 1 1	Ω Ω Ω
t _{PHL}	Turn-on Delay	I _O = 500mA No Reactive Load			10	μs
t _P	Turn-off Delay	I _O = 500mA No Reactive Load			10	μs
V _{OREF}	Fault Refer. Voltage	Output Progr. OFF Fault detected if V _O > V _{OREF}	1.6		2	V
t _{UD}	Fault Reset Delay (after CE L to H transition)	See fig. 3	75		250	μs
V _{OFF}	Output OFF Voltage	Output Pin Floating.cOutput Progr. OFF,			1.0	V

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INPUT BUFFER (SI, CE, SCLK and RESET pins)						
V_{T-}	Threshold Voltage at Falling Edge		$0.2V_{CC}$			V
V_{T+}	Threshold Voltage at Rising Edge				$0.7V_{CC}$	V
V_H	Hysteresis Voltage	$V_{T+} - V_{T-}$		1.45		V
I_I	Input Current	$V_{CC} = 5.25V, 0 < V_I < V_{CC}$	- 10		+ 10	μA
C_I	Input Capacitance	$0 < V_I < V_{CC}$			20	pF

OUTPUT BUFFER (SO pin)

V_{SOL}	Output LOW Voltage	$I_O = 1.6mA$			0.4	V
V_{SOH}	Output HIGH Voltage	$I_O = 0.8mA$	$V_{CC} - 1.3V$			V
I_{SOI}	Output Tristate Leakage Current	$0 < V_O < V_{CC}, CE$ Pin Held High, $V_{CC} = 5.25V$	- 10		10	μA
C_{SO}	Output Capacitance	$0 < V_O < V_{CC}$ CE Pin Held High			20	pF
I_{CC}	Quiescent Supply Current at V_{CC} Pin	All Outputs Progr. ON. $I_O = 0.5A$ per Output Simultaneously			10	mA

SERIAL PERIPHERAL INTERFACE (see fig. 2, timing diagram)

f_{op}	Operating Frequency		D.C.		2	MHz
t_{lead}	Enable Lead Time		250			ns
t_{lag}	Enable Lag Time		250			ns
t_{wSCKH}	Clock HIGH Time		200			ns
t_{wSCKL}	Clock LOW Time		200			ns
t_{su}	Data Setup Time		75			ns
t_H	Data Hold Time		75			ns
t_{EN}	Enable Time				250	ns
t_{DIS}	Disable Time				250	ns
t_V	Data Valid Time				100	ns
t_{rSO}	Rise Time (SO output)	$V_{CC} = 20$ to 70% $C_L = 200pF$			50	ns
t_{fSO}	Fall Time (SO output)	$V_{CC} = 70$ to 20% $C_L = 200pF$			50	ns
t_{rSI}	Rise Time SPI Inputs (SCK, SI, CE)	$V_{CC} = 20$ to 70% $C_L = 200pF$			200	ns
t_{fSI}	Fall Time SPI Inputs (SCLK, SI, CE)	$V_{CC} = 70$ to 20% $C_L = 200pF$			200	ns
t_{ho}	Output Data Hold Time		0			ns

FUNCTIONAL DESCRIPTION

The L9822N DMOS output is a low operating power device featuring, eight 1Ω $R_{DS(ON)}$ DMOS drivers with transient protection circuits in output stages. Each channel is independently controlled by an output latch and a common RESET line which disables all eight outputs. The driver has low saturation and short circuit protection and can drive inductive and resistive loads such as solenoids, lamps and relays. Data is transmitted to the device serially using the Serial Peripheral Interface (SPI) protocol. The circuit receives 8 bit serial data by means of the serial input (SI) which is stored in an internal register to control the output drivers. The serial output (SO) provides 8 bit of diagnostic data representing the voltage level at the driver output. This allows the microprocessor to diagnose the condition of the output drivers.

The output saturation voltage is monitored by a comparator for an out of saturation condition and is able to unlatch the particular driver through the fault reset line. This circuit is also cascadable with another octal driver in order to jam 8 bit multiple data. The device is selected when the chip enable (CE) line is low.

Additionally the (SO) is placed in a tri-state mode when the device is deselected. The negative edge of the (CE) transfers the voltage level of the drivers to the shift register and the positive edge of the (CE) latches the new data from the shift register to the drivers. When CE is Low, data bit contained into the shift register is transferred to SO output at every SCLK positive transition while data bit present at SI input is latched into the shift register on every SCLK negative transition.

Internal Blocks Description

The internal architecture of the device is based on the three internal major blocks : the octal shift register for talking to the SPI bus, the octal latch for holding control bits written into the device and the octal load driver array.

Shift Register

The shift register has both serial and parallel inputs and serial and parallel outputs. The serial input accepts data from the SPI bus and the serial output simultaneously sends data into the SPI bus. The parallel outputs are latched into the parallel latch inside the L9822N at the end of a data transfer. The parallel inputs jam diagnostic data into the shift register at the beginning of a data transfer cycle.

Parallel Latch

The parallel latch holds the input data from the shift register. This data then actuates the output stages.

Individual registers in the latch may be cleared by fault conditions in order to protect the overloaded output stages. The entire latch may also be cleared by the RESET signal.

Output Stages

The output stages provide an active low drive signal suitable for 0.75A continuous loads. The outputs have internal zeners set to 36 volts to clamp inductive transients at turn-off. Each output also has a voltage comparator observing the output node. If the voltage exceeds 1.8V on an ON output pin, a fault condition is assumed and the latch driving this particular stage is reset, turning the output OFF to protect it. The timing of this action is described below. These comparators also provide diagnostic feedback data to the shift register. Additionally, the comparators contain an internal pulldown current which will cause the cell to indicate a low output voltage if the output is programmed OFF and the output pin is open circuited.

TIMING DATA TRANSFER

Figure #2 shows the overall timing diagram from a byte transfer to and from the L9822NSP using the SPI bus.

CE High to Low Transition

The action begins when the Chip Enable (CE) pin is pulled low. The tri-state Serial Output (SO) pin driver will be enabled entire time that CE is low. At the falling edge of the CE pin, the diagnostic data from the voltage comparators in the output stages will be latched into the shift register. If a particular output is high, a logic one will be jammed into that bit in the shift register. If the output is low, a logic zero will be loaded there. The most significant bit (07) should be presented at the Serial Input (SI) pin. A zero at this pin will program an output ON, while a one will program the output OFF.

SCLK Transitions

The Serial Clock (SCLK) pin should then be pulled high. At this point the diagnostic bit from the most significant output (07) will appear at the SO pin. A high here indicates that the 07 pin is higher than 1.8V. The SCLK pin should then be toggled low then high. New SO data will appear following every rising edge of SCLK and new SI data will be latched into the L9822N shift register on the falling edges. An unlimited amount of data may be shifted through the device shift register (into the SI pin and out the SO pin), allowing the other SPI devices to be cascaded in a daisy chain with the L9822N.

CE Low to High Transition

Once the last data bit has been shifted into the L9822NSP, the CE pin should be pulled high.

At the rising edge of CE the shift register data is latched into the parallel latch and the output stages will be actuated by the new data. An internal 160µs delay timer will also be started at this rising edge (see t_{UD}). During the 160µs period, the outputs will be protected only by the analog current limiting circuits since the resetting of the parallel latches by faults conditions will be inhibited during this period. This allows the part to overcome any high inrush currents that may flow immediately after turn on. Once the delay period has elapsed, the output voltages are sensed by the comparators and any output with voltages higher than 1.8V are latched OFF. It should be noted that the SCLK pin should be low at both transitions of the CE pin to avoid any false clocking of the shift register. The SCLK input is gated by the

CE pin, so that the SCLK pin is ignored whenever the CE pin is high.

FAULT CONDITIONS CHECK

Checking for fault conditions may be done in the following way. Clock in a new control byte. Wait 160 microseconds or so to allow the outputs to settle. Clock in the same control byte and observe the diagnostic data that comes out of the device. The diagnostic bits should be identical to the bits that were first clocked in. Any differences would point to a fault on that output. If the output was programmed ON by clocking in a zero, and a one came back as the diagnostic bit for that output, the output pin was still high and a short circuit or overload condition exists. If the output was programmed OFF by clocking in a one, and a zero came back as the diagnostic bit for that output, nothing had pulled the output pin high and it must be floating, so an open circuit condition exists for that output.

Figure 1 : Byte Timing with Asynchronous Reset.

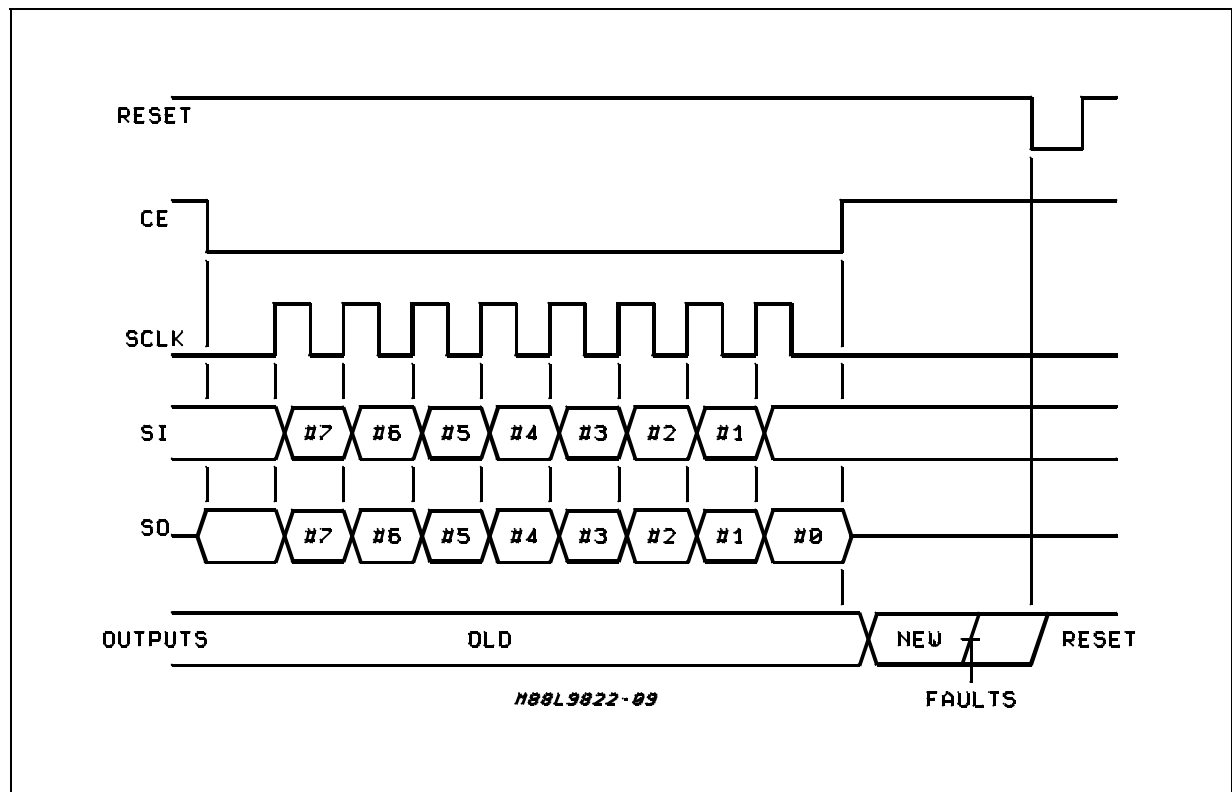


Figure 2 : Timing Diagram.

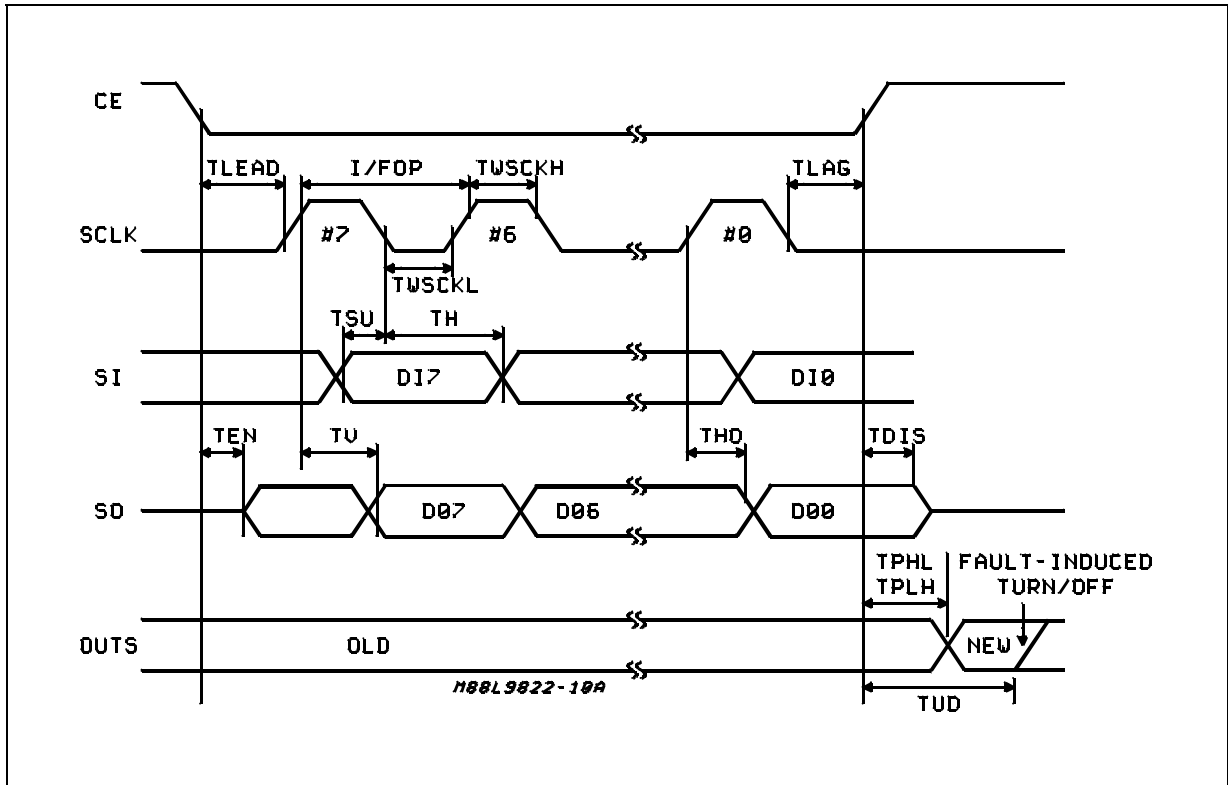
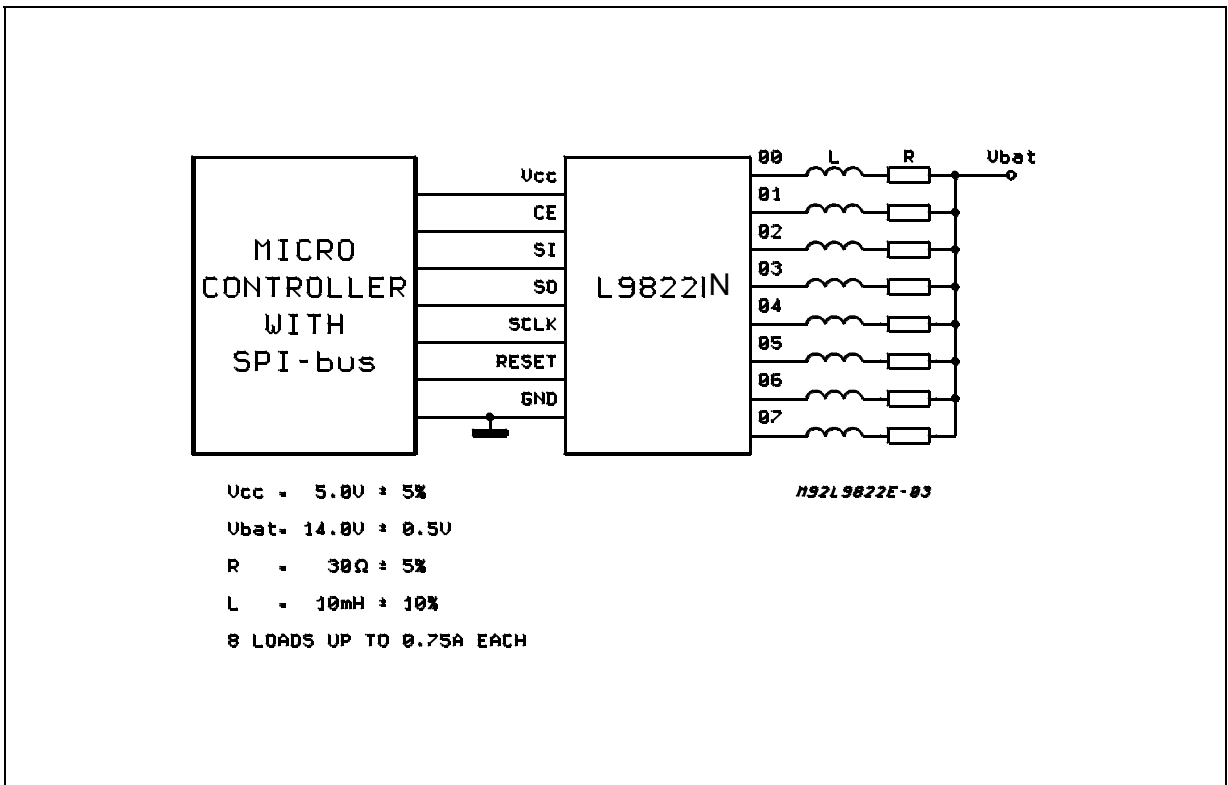


Figure 3 : Typical Application Circuit.

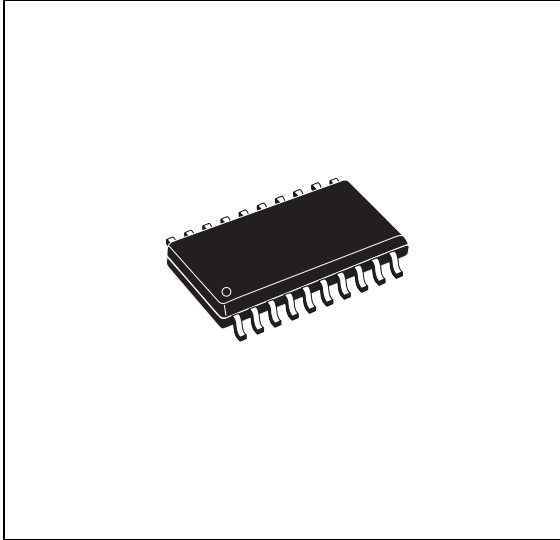


L9822N

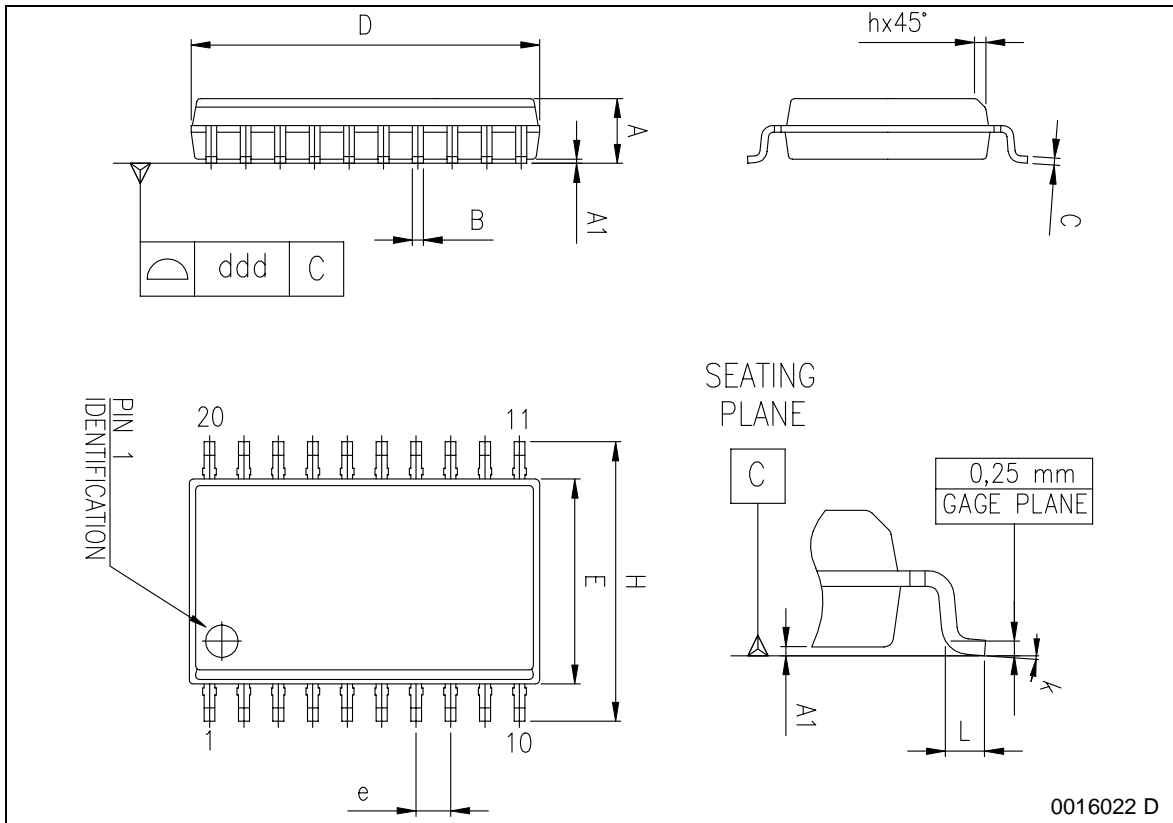
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	12.60		13.00	0.496		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA



SO20



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