Ordering number : EN4946A

Monolithic Digital IC

SANYO No. 4946A

LB8108M

Actuator Driver for Portable CD Players

Applications

The LB8108M is an actuator driver for use in portable CD players that operate at a power supply voltage of 2.4 (two nicad batteries) or 3.0 V (two dry-cell batteries).

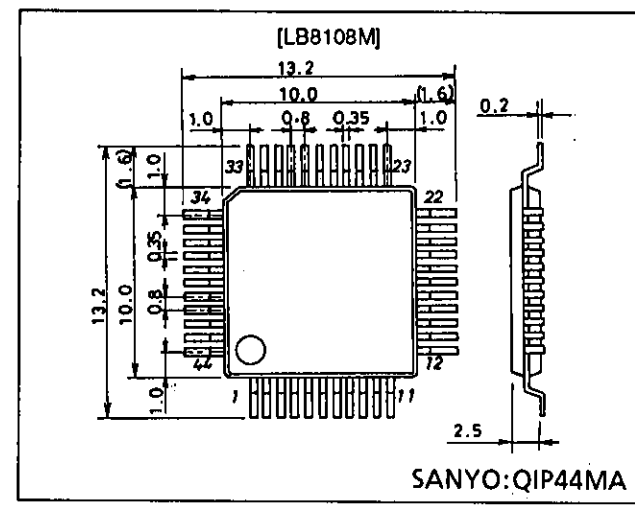
Functions and Features

- Includes four H bridge driver channels to drive the four CD player actuators (focus coil, tracking coil, spindle motor and sled motor).
  (output dynamic range: maximum of about 2 V)
- Includes a 3.9 V (typical) step-up circuit to supply the DSP, ASP and microprocessor used in the CD player. Also includes another voltage step-up circuit whose voltage can be set with external resistors.
  (However, note that the transistors, inductors, capacitors and diodes required for drive operation are all external components.)
- Built-in oscillator circuit for these converters
  (external resistor and capacitor required)
- Detects the maximum value of the four driver outputs and supplies a voltage slightly higher than that voltage to the H bridge block in each of the four channels using PWM voltage converter. This allows a drive scheme with extremely low loss to be implemented.
  (However, note that the pnp transistor, inductor, capacitor, and diodes for the PWM circuit are all external components.)
- Built-in laser diode drive and APC circuits
  ($I_O$max ≈ 100 mA. This function can be turned off by a control voltage input. It is composed of step-up converter and series regulator.
  However, note that the transistors, inductors, capacitors and diodes required for drive operation are all external components.)
- The sled motor drive circuit operates in 2 modes, that are normal V-type drive mode and step drive mode which is highly effective in reducing power dissipation.
- A step-down converter that convert external input voltage that exceed 5 V into 3.5 V V_{CC} operates when an external voltage input is applied. This simplifies power supply design and thermal design for applying V_{CC}.
  (This circuit turns on at the same time an external voltage is applied and generates a 3.5 V V_{CC}, which is utilize for nicad battery charging.)
- Built-in microprocessor reset circuit (external capacitor required)
  (This circuit detects the V_{CD} pin voltage and operates a reset voltage with an H-side of 2.2 V (typical) and an L-side of 2.1 V (typical).)
- Two built-in battery check comparator channels
- System start and stop under microprocessor control
- Actuator muting function included.
  (all four channels at the same time)
- Built-in thermal shutdown circuit

Package Dimension

unit: mm

3148-QFP44MA



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Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7	V
External input voltage	V_{EXT} max		9	V
H bridge output current	I_{OUT} max	Taking 400 mA per channel as the maximum.	800	mA
Step-up circuit output current	I_{CD} max		150	mA
Allowable power dissipation	Pd max	Independent IC	900	mW
Operating temperature	Topr		−20 to +75	°C
Storage temperature	Tstg		−55 to +150	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		1.6 to 3.5	V
External input voltage	V_{EXT}		5.0 to 8.0	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 3 V

Parameter	Symbol	Conditions	min	typ	max	Unit
[Power Supply Block]						
Standby current drain	I_{CCO}	S/S = high			100	μA
Quiescent current	I_{CC}	S/S = low, with no drive input		16	25	mA
[Step-up Circuit (3.9 V)]						
Step-up output voltage	V_{CD}		3.7	3.9	4.1	V
NPN drive current	$I_{D\ CD}$			3.0		mA
Load regulation	$R_{LD\ CD}$				1000	mV/A
Line regulation	$R_{LN\ CD}$				100	mV/V
Minimum off duty	$D_{MIN\ CD}$			50		%
[Externally Set Step-Up Circuit]						
NPN drive current	$I_{D\ UP}$			3.0		mA
Input bias current	$I_{B\ UP}$				200	nA
Minimum off duty	$D_{MIN\ UP}$			50		%
[H Bridge Output Block, PWM Block]						
Output saturation voltage	$V_{H\ sat}$	I_O = 200 mA, TOP + BOTTOM		0.30	0.45	V
Maximum output voltage	V_{PWM} max			2.25		V
PNP drive current	$I_{D\ PWM}$			V_{OUT}/600		mA
Load regulation	$R_{LD\ PWM}$				1000	mV/A
Line regulation	$R_{LN\ PWM}$				100	mV/V
[Drive Control Block]						
Input bias current	$I_{B\ IN}$				2.0	μA
ASP reference input voltage range	V_{ASPR}		1.2		V_{CD} − 1.3	V
Transfer gain	G_{IN}	For R_L = 10 Ω		7.95		dB
Transfer gain difference (+/-)	ΔG_{IN}	For R_L = 10 Ω	−1.0	0	+1.0	dB
Input dead zone voltage	V_{DZ}		−30	0	+30	mV
[Sled Drive Circuit]						
SLREF input voltage range	V_{SLREF}				V_{CD} − 0.5	V
Input bias current	$I_{B\ SLED}$				200	nA
SLM on voltage	V_{SLM}		2.0			V
[Oscillator Block]						
Oscillator power output voltage	V_{OSCP}		V_{CC} − 0.15			V
Oscillator maximum frequency	F_{MAX}				100	kHz
OSC pin input bias current	$I_{B\ OSC}$		−2.0			μA

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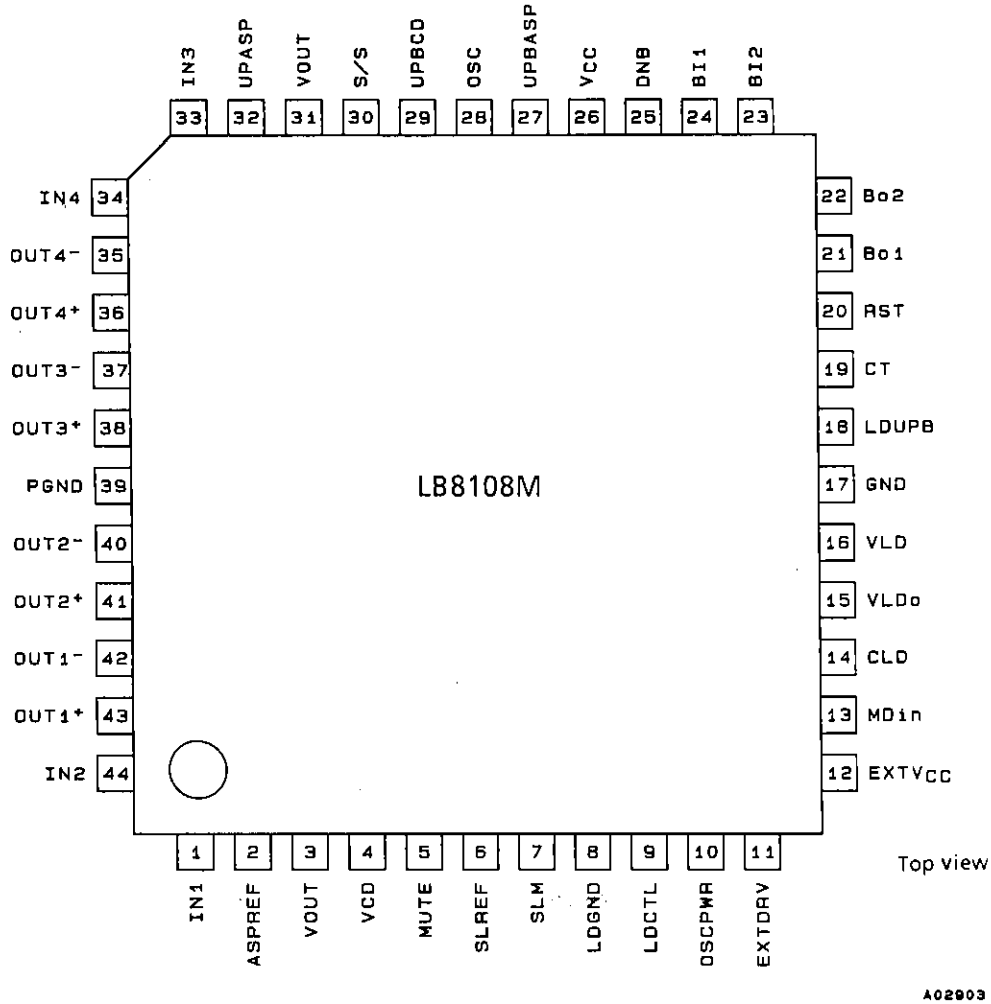
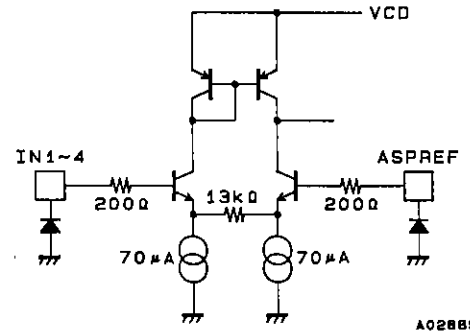
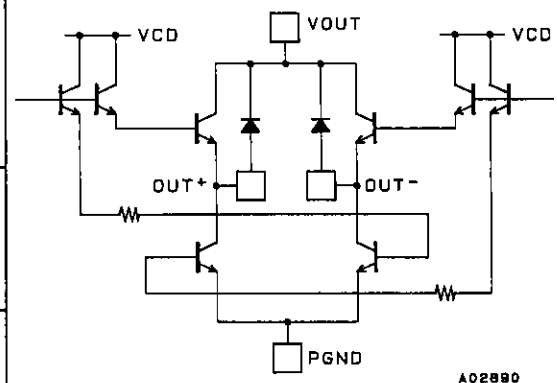
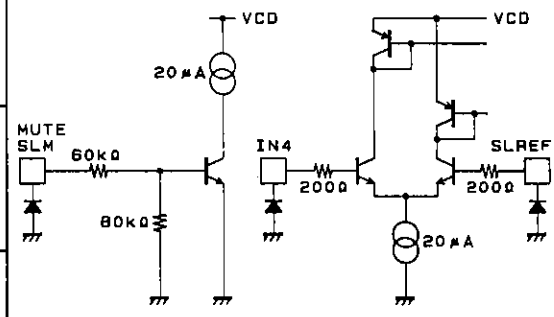
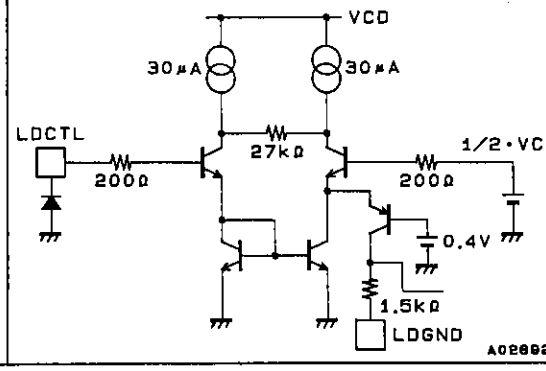
Parameter	Symbol	Conditions	min	typ	max	Unit
[Battery Check Block]						
BI1 and BI2 input bias current	$I_{B\ BI1,2}$				200	nA
BO1 and BO2 output saturation voltage	$V_{BO1,2}$	For I_O = 500 µA			0.3	V
[S/S Pin Function]						
S/S start voltage	$V_{SS\ ON}$				V_{CC} – 1.0	V
S/S off voltage	$V_{SS\ OFF}$		V_{CC} – 0.5			V
[External Voltage Input Block]						
Minimum operating input voltage	$V_{I\ EXT}$		5.0			V
PNP drive current	$I_{D\ EXT}$			3.0		mA
Step-down circuit output voltage	$V_{O\ EXT}$		3.3	3.5	3.7	V
[Muting Block]						
Muting on voltage	V_{MUTE}		2.0			V
[APC Circuit Block]						
Maximum output current	$I_{O\ APC}$			100		mA
LDCTL pin input bias current	$I_{B\ LDC}$		–5.0			µA
LDCTL off voltage	V_{LDOFF}			0.4		V
MDin pin input bias current	$I_{B\ MDIN}$		–1.0			µA
VLD step-up voltage	V_{LDOUT}	Taking V_{LDO} as the reference		0.3		V
NPN drive current	$I_{D\ LDO}$			1.0		mA
[Reset Circuit Block]						
Reset charge current	I_{CHG}			–1.25		µA
Output saturation voltage	V_{RST}	For I_O = 100 µA			0.3	V
H side detection voltage	V_{HSENSE}	For the V_{CD} pin voltage*1	2.1	2.2	2.3	V
L side detection voltage	V_{LSENSE}	For the V_{CD} pin voltage*1	2.0	2.1	2.2	V
[TSD Block]						
TSD operating temperature	T_{TSD}	Design target value*2		180		°C
TSD temperature hysteresis	ΔT_{TSD}	Design target value*2		20		°C

Note: 1. V_{HSENSE} and V_{LSENSE} will never be inverted in any individual IC.
2. Items specified to be a design target value in the conditions column are not measured.

Pin Assignment



Pin Functions

Pin No.	Symbol	Equivalent circuit	Function
1, 44 33, 34 2	IN1, IN2 IN3, IN4 ASPREF		The actuator control signals corresponding to IN1: focus, IN2: tracking, IN3: spindle, IN4: sled. Input from the ASP (DSP).
43, 42 41, 40 38, 37 36, 35	OUT1+, 1– OUT2+, 2– OUT3+, 3– OUT4+, 4–		Focus coil actuator drive output Tracking coil actuator drive output Spindle motor drive output Sled motor drive output (Each channel includes built-in spark killer diodes.)
3, 31	V_{OUT}		Power supply for the four H bridge driver channels. An external PWM step-up circuit can be used to generate a voltage slightly higher than the maximum voltage output by any of the four output channels.
4	V_{CD}		Input for the 3.9 V step-up circuit. The drive control system operates on this voltage. This voltage can also be supplied to other ICs in the system, such as the DSP and the microprocessor.
5	MUTE		Input for muting of the four actuator channels at the same time. High: mute applied.
6	SLREF		Threshold input used when operating the sled motor in step drive mode.
7	SLM		Input that selects sled motor step drive mode. High: V-type selected Low: Step mode
8	LD GND		Dedicated ground connection for the internal reference voltage for laser diode APC control. Connect to a ground near the laser diode.

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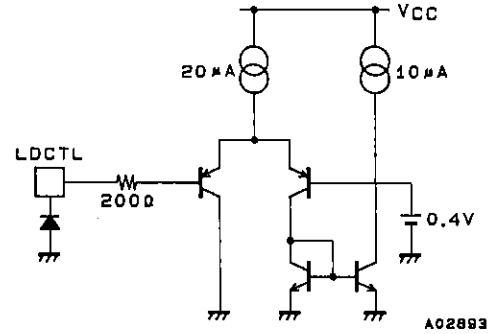
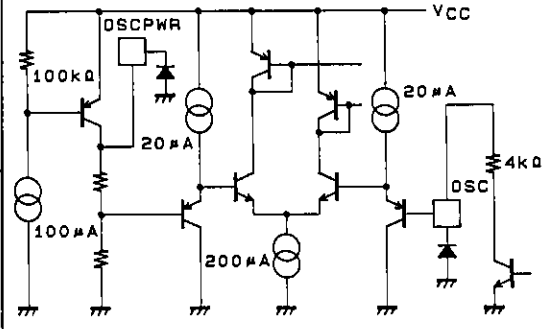
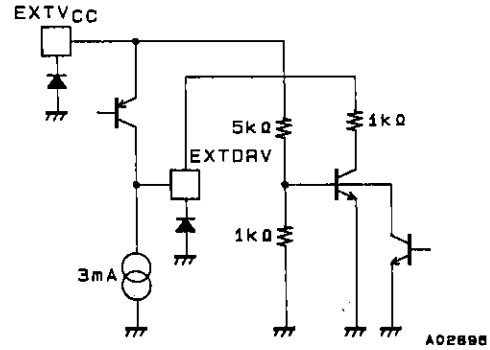
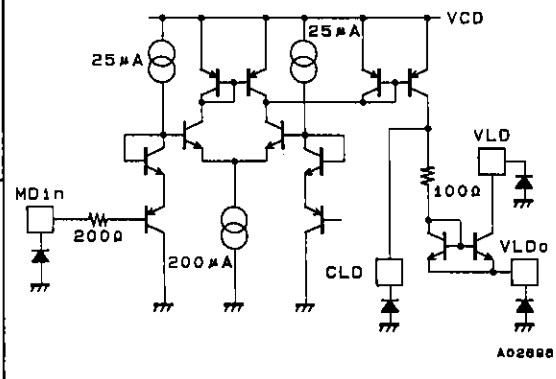
Pin No.	Symbol	Equivalent circuit	Function
9	LDCTL		Laser diode APC (auto power control) control signal input. When this voltage falls under about 0.4 V the APC output is turned off.
10	OSCPWR		RC power supply for invalid current prevention for the OSC oscillator circuit.
28	OSC		Input for the free-running oscillator circuit used for PWM step-down and step-up circuits. The oscillator frequency is determined by an external RC circuit.
11	EXTDRV		Base drive output for external step-down pnp transistor used when external power is applied.
12	$EXTV_{CC}$		External power supply input. This voltage is converted into 3.5 V with a PWM step-down circuit and supplied to V_{CC}.
13	MD in		Input for the output from the laser diode APC monitor diode.
14	C_{LD}		Terminal for the capacitor that eliminates high frequency from laser drive signal. This capacitor is also useful for soft starting in the LD output.

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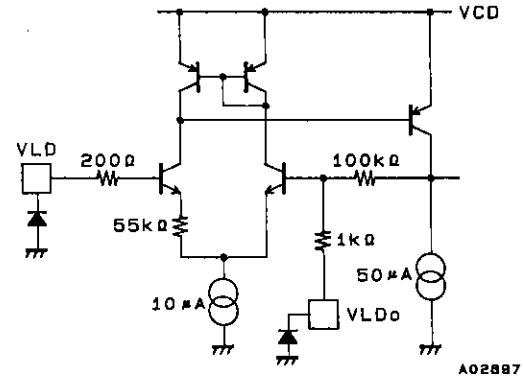
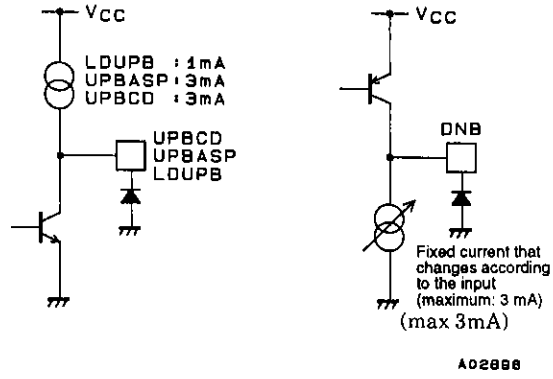
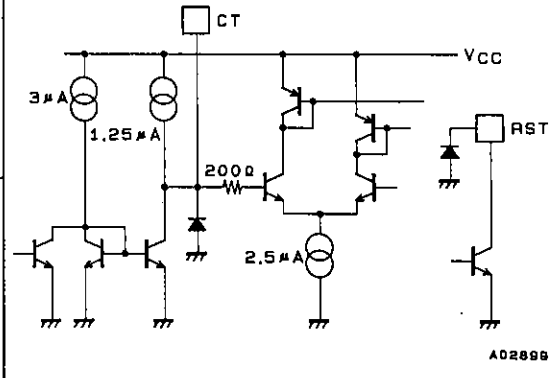
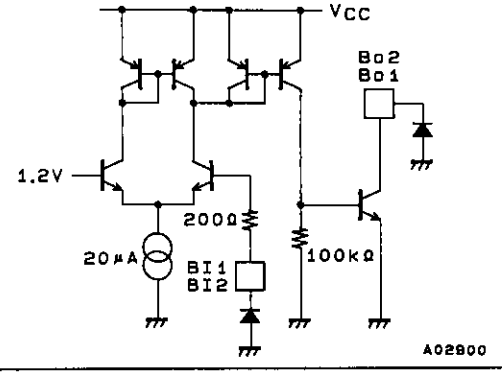
Pin No.	Symbol	Equivalent circuit	Function
15	V_{LDO}		Output that directly drives the laser diode. I_O max is about 100 mA.
16	V_{LD}		Input in the laser APC circuit for the external step-up circuit used to assure V_{LDO} (i.e., to assure V_{CE} for the internal output transistor) when V_{CC} falls. V_{LD} is controlled to 0.3 V (typical) more than V_{LDO}.
17	GND		LB8108M small signal system ground (ground for circuits without the output transistor)
18	LDUPB		Base drive circuit for external step-up npn transistor in the laser APC circuit for the external step-up circuit used to assure V_{LDO} when V_{CC} falls.
25	DNB		Base drive output for the step-down PWM pnp transistor that generates the power supplied to the actuator H bridge drivers.
27	UPBASP		Base drive output for the external npn transistor for the step-up circuit whose step-up voltage is set externally.
29	UPBCD		Base drive output for the 3.9 V step-up external npn transistor.
19	CT		Terminal for the reset circuit capacitor (The reset time will be about 50 ms for a 0.1 μF capacitor.)
20	RST		Reset circuit open collector output
21, 22	BO1, BO2		Battery check comparator open collector output
24, 23	BI1, BI2		Battery check comparator input. This voltage is compared to 1.2 V internally.

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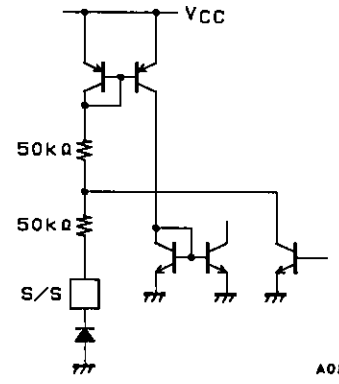
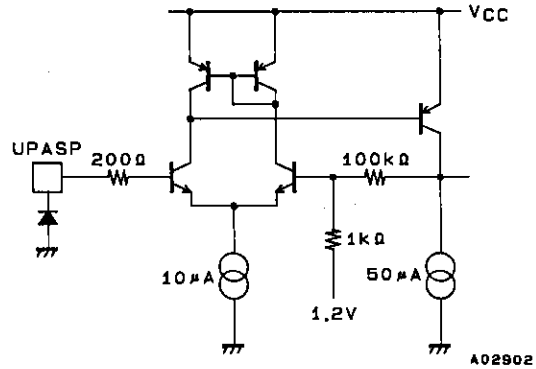
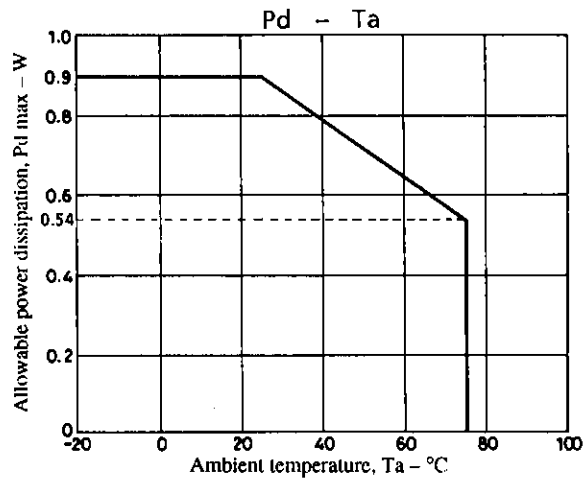
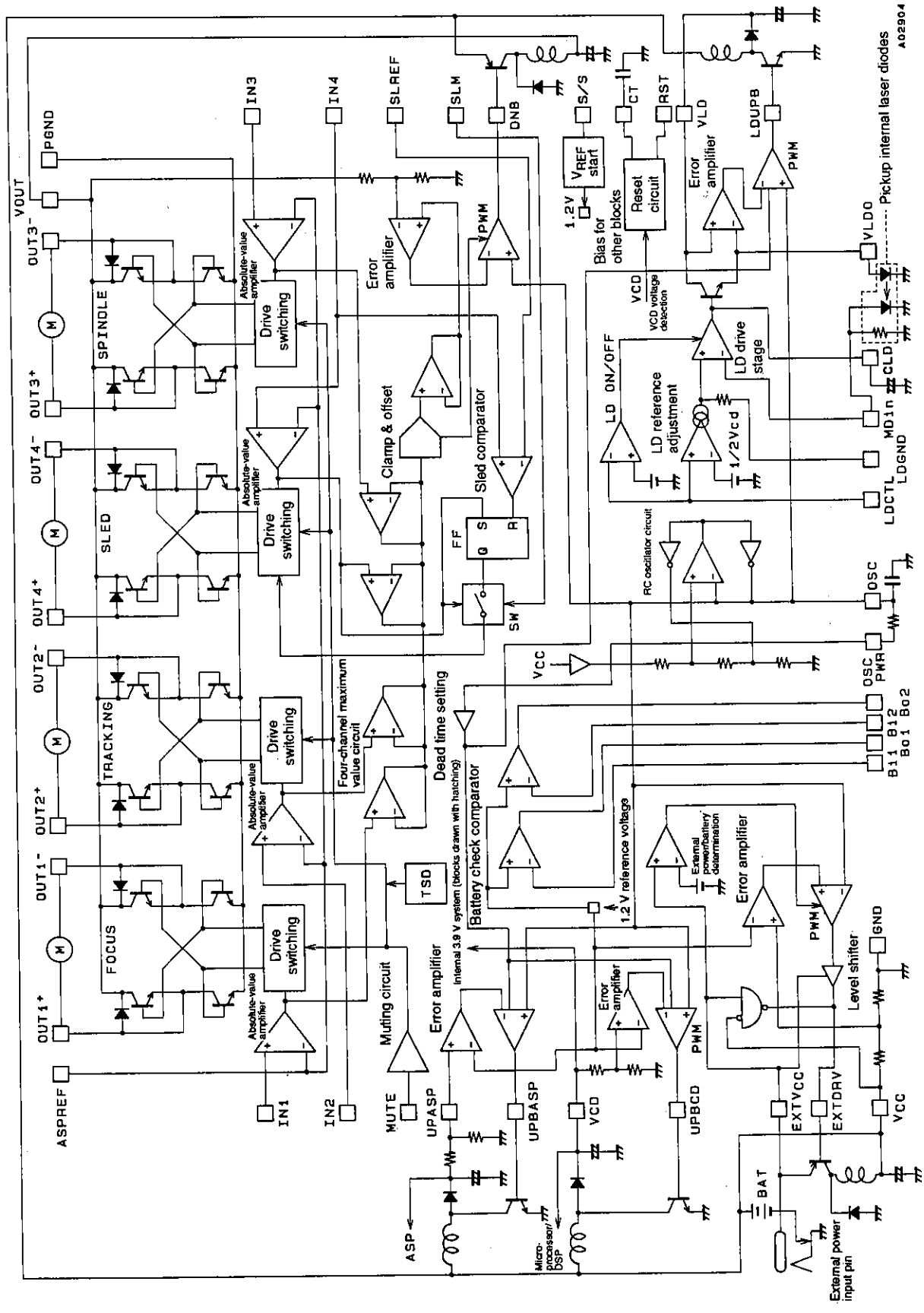
Pin No.	Symbol	Equivalent circuit	Function
26	V_{CC}		Power supply connection
30	S/S		LB8108M start input (starts on a low level input). No power on lock function is included.
32	UPASP		Voltage feedback input for the externally set step-up circuit. The step-up voltage is determined by comparing this voltage to 1.2 V.
39	PGND		Ground for the four H bridge driver channel output transistors. This ground is not connected to the small signal system ground internally.



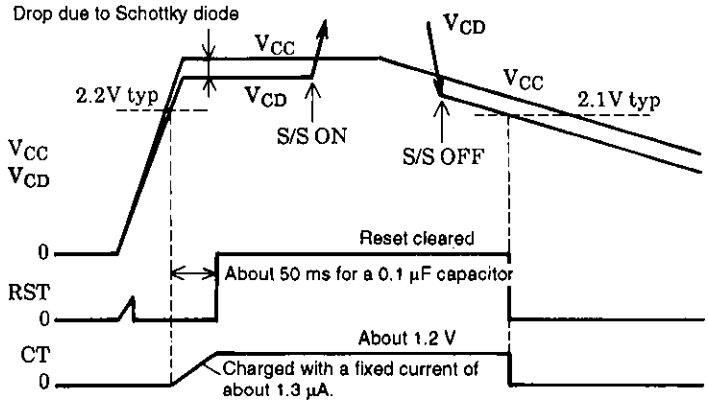
Block Diagram



Operating Description

Reset Function

The LB8108M includes a built-in circuit that outputs a reset signal to the control microprocessor. This circuit operates when V_{CC} is applied. (It does not depend on the S/S circuit.)
The reset time is determined by the capacitor connected to the CT pin, and will be about 50 ms for a 0.1 μF capacitor.
The level detection circuit detects the V_{CD} voltage as shown in the figure.

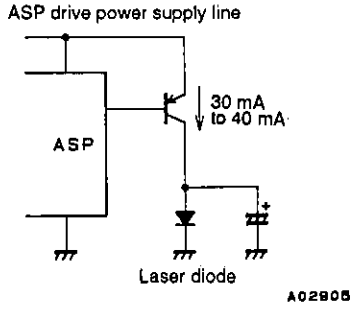


That is, the reset state is cleared by RST going from low to high after the passage of the time determined by CT starting at the point the V_{CD} voltage exceeds 2.2 V (typical) after V_{CC} is applied. At this time RST will remain cleared even if S/S is turned on and V_{CD} rises to 3.9 V (typical). Then, if S/S is turned off and the V_{CD} voltage returns to the voltage determined by V_{CC} and the Schottky diode voltage drop, and additionally, the V_{CD} voltage falls under 2.1 V (typical) due to a drop in the battery voltage, reset is applied (turned on) again.
(In other words, there is hysteresis in the detection level.)
(Note that since the RST output has a limited drive current, it should be used with a pull-up resistor of about 100 kΩ.)

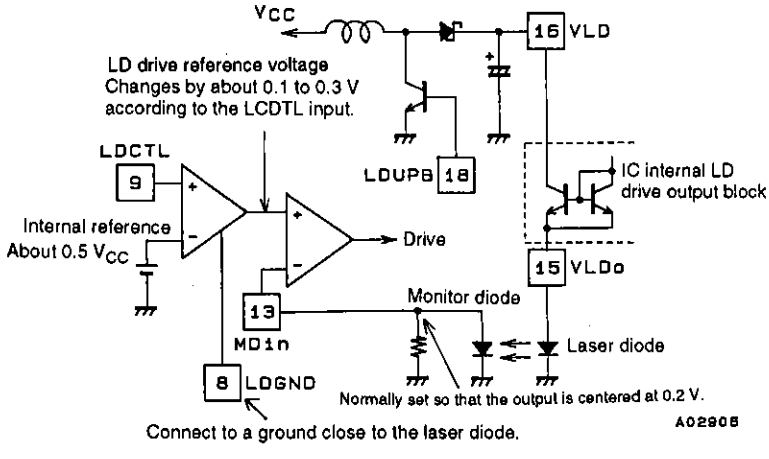
APC Function

In systems that used earlier drivers, the laser diode APC (auto power control) circuit that adopted an ASP (analog signal processor) were generally used. However, this ASP was originally driven by the power supply stepped up from V_{CC} by the driver IC and the laser diode was then driven by a series type regulator supplied by that voltage. This had the problem that the power dissipation was large.
This power dissipation takes a large part of the total power dissipation in the whole system, especially in portable equipment. To reduce this power dissipation, the LB8108M takes the power for the laser diode directly from V_{CC}.
(In practice, this circuit consists of an up converter and a series regulator. When the V_{CC} voltage is high enough, the circuit operates as a series type circuit, but since these circuits are expected to be used in portable applications, that will be relatively rare.)

Laser Diode Drive Technique in General



Overview of the LB8108M Laser Diode Drive System



First, when V_{CC} is adequately high (about 2.5 V or over) the laser diode is driven by the system consisting of V_{CC}, an inductor and a Schottky diode without driving LDUPB. Then, when V_{CC} falls and $V_{LD} - V_{LDO}$ become under about 0.3 V, LDUPB is driven, V_{LD} is stepped up, and the circuit is controlled so that $V_{LD} - V_{LDO}$ is held at 0.3 V (typical).

The following describes the laser diode intensity adjustment function supported by the LB8108M.
First, set up the pickup so that the monitor diode output is about 0.2 V in the normal usage range.
When LDCTL is in the range 0.0 to 0.5 V the LD drive function will be in the cutoff state and the laser diode will not be driven. As the LDCTL voltage rises, the LD drive reference voltage shown in the figure varies between 0.1 and 0.3 V. Then, the V_{LDO} pin voltage is controlled so that the monitor diode output and that reference voltage become identical. However, since the output current peak is 100 mA (typical), the output voltage will not increase when an output current in excess of that value is required.
(Since the intensity adjustment will go to its maximum setting when the LDCTL pin is open, an appropriate voltage must be applied to the LDCTL pin.)

Sled Control

The figure below shows the operation of the LB8108M's sled actuator step control.

When the SLM pin is set high, the LB8108M operates in the normal V-type control mode. However, the LB8108M can be set to operate in a sled drive mode that is highly efficient at reducing power dissipation by setting the SLM pin low.
The step drive start level is input from the SLREF pin. (Only a voltage higher than V_{ASPREF} will be accepted.)
The circuit operates once in step drive mode following the locus of line ① in the figure. Then, on returning, it operates in V-type control following the locus of line ②.
Next, the circuit can be operated in step mode by putting the input ($V_{IN}4$) into the reverse region.
(If the input does not enter the reverse region, the circuit will continue to operate in V-type mode.)