

RMWB11001

11 GHz Buffer Amplifier MMIC

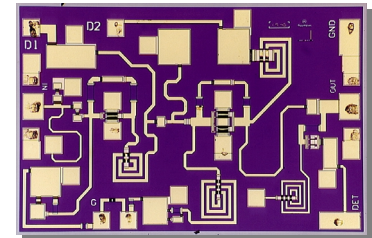
PRODUCT INFORMATION

Description

The RMWB11001 is a 2-stage GaAs MMIC amplifier designed as a 10.5 to 11.7 GHz Buffer Amplifier for use in the LO chain of point to point radios, point to multi-point communications, LMDS, and other millimeter wave applications. In conjunction with other Raytheon amplifiers, multipliers and mixers it forms part of a complete 38 GHz transmit/receive chipset. The RMWB11001 utilizes Raytheon's 0.25µm power PHEMT process and is sufficiently versatile to serve in a variety of medium power amplifier applications.

Features

- ◆ 4 mil substrate
- ◆ Small-signal gain 21 dB (typ.)
- ◆ Saturated power out 19 dBm (typ.)
- ◆ Voltage detector included to monitor Pout
- ◆ Chip size 2.0 mm x 1.3 mm



Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Positive DC voltage (+4 V Typical)	Vd	+6	Volts
Negative DC voltage	Vg	-2	Volts
Simultaneous (Vd - Vg)	Vd _g	8	Volts
Positive DC Current	I _D	104	mA
RF Input Power (from 50 Ω source)	P _{IN}	+8	dBm
Operating Baseplate Temperature	T _C	-30 to +85	°C
Storage Temperature Range	T _{stg}	-55 to +125	°C
Thermal Resistance (Channel to Backside)	R _{jc}	180	°C/W

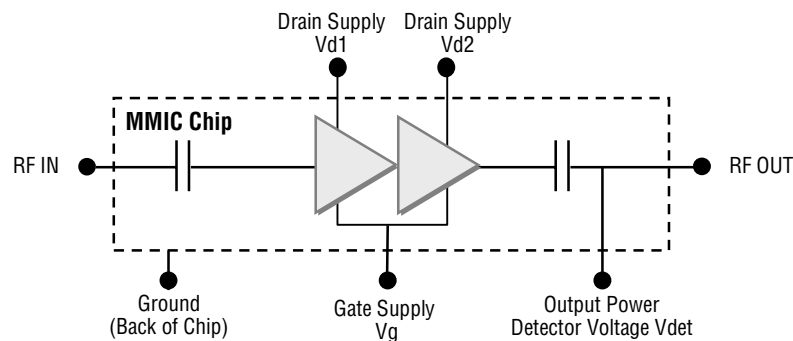
Electrical Characteristics

(At 25°C), 50 Ω system, Vd=+4 V, Quiescent Current Idq=36 mA

Parameter	Min	Typ	Max	Unit
Frequency Range	10.5		11.7	GHz
Gate Supply Voltage ¹ (Vg)		-0.5		V
Gain Small Signal (Pin=-10 dBm)	18	21		dB
Gain Variation vs. Frequency		0.5		dB
Power Output Saturated: (Pin=2 dBm)	17	19		dBm
Drain Current at Psat (Pin=2 dBm)		55		mA

Parameter	Min	Typ	Max	Unit
Power Added Efficiency (PAE): at Psat		35		%
Input Return Loss (Pin=-10 dBm)		13		dB
Output Return Loss (Pin=-10 dBm)		18		dB
Noise Figure		4		dB
Detector Voltage (Pout=+18 dBm)		0.5		V

Functional Block Diagram²



Notes:

1. Typical range of gate voltage is -0.8 to -0.2V to set Idq of 36 mA.
2. Detector delivers approx. 0.5V DC into 3k Ω load resistor for >+18 dBm output power. If output power level detection is not desired, do not make connection to detector bond pad.

Characteristic performance data and specifications are subject to change without notice.

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Figure 1

Chip Layout and Bond Pad Locations

Chip Size is 2.0 mm x 1.3 mm x 100 μm .
Back of chip is RF and DC ground

Dimensions in mm

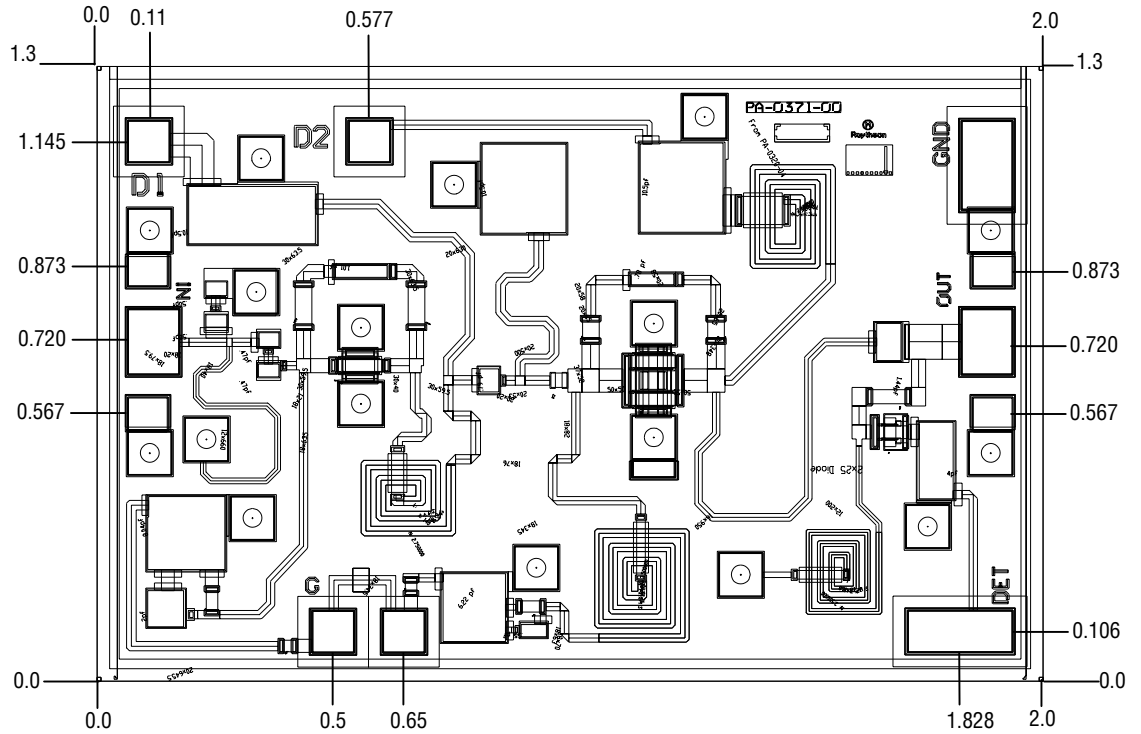
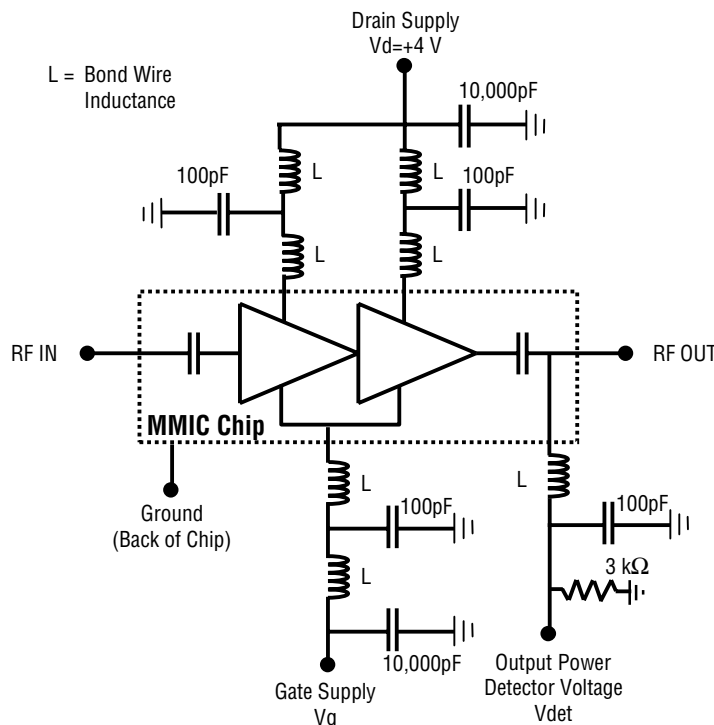


Figure 2

Recommended Application Schematic Circuit Diagram



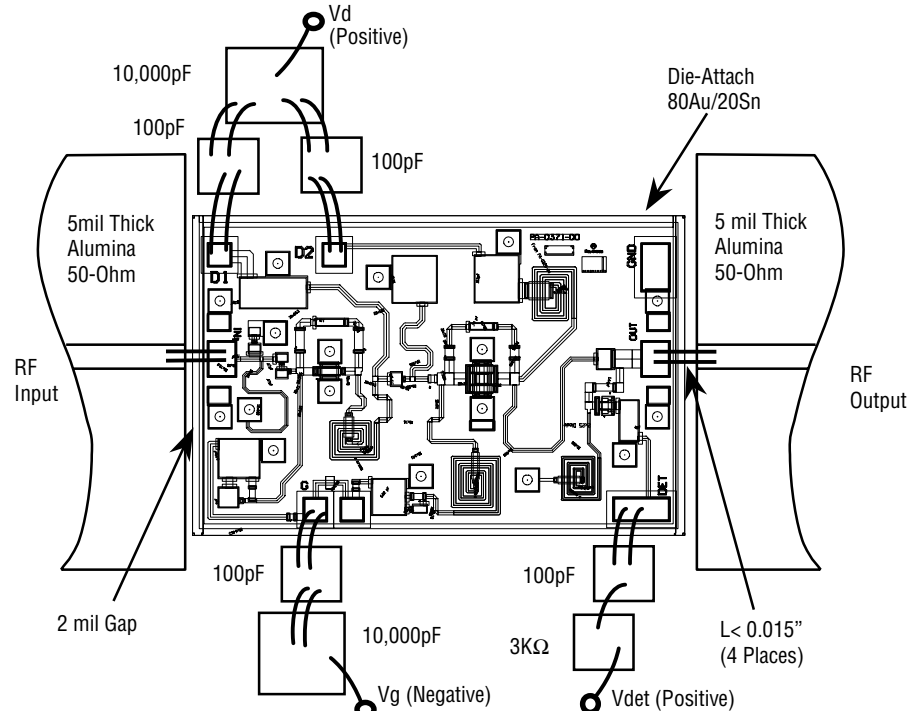
Note: Detector delivers approx. 0.5V DC into 3k Ω load resistor for $>+18$ dBm output power. If output power level detection is not desired, do not make connection to detector bond pad.

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Figure 3
Recommended
Assembly Diagram



Notes:

Use 0.003" by 0.0005" Gold Ribbon for bonding. RF input and output bonds should be less than 0.015" long with stress relief.

Detector delivers approx. 0.5V DC into 3 k Ω load resistor for >+18 dBm output power. If output power level detection is not desired, do not make connection to detector bond pad.

Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF and DC ground.

These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses 3 mils wide and 0.5 mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 0.012" long corresponding to a typically 2 mil between the chip and the substrate material.

Recommended Procedure for Biasing and Operation

CAUTION: LOSS OF GATE VOLTAGE (VG) WHILE DRAIN VOLTAGE (VD) IS PRESENT MAY DAMAGE THE AMPLIFIER CHIP.

The following sequence of steps must be followed to properly test the amplifier:

Step 1: Turn off RF input power.

Step 2: Connect the DC supply grounds to the grounds of the chip carrier.
Slowly apply negative gate bias supply voltage of -1.5 V to Vg.

Step 3: Slowly apply positive drain bias supply voltage of +4 V to Vd.

Step 4: Adjust gate bias voltage to set the quiescent current of Idq=36 mA.

Step 5: After the bias condition is established, RF input signal may now be applied at the appropriate frequency band.

Step 6: Follow turn-off sequence of:

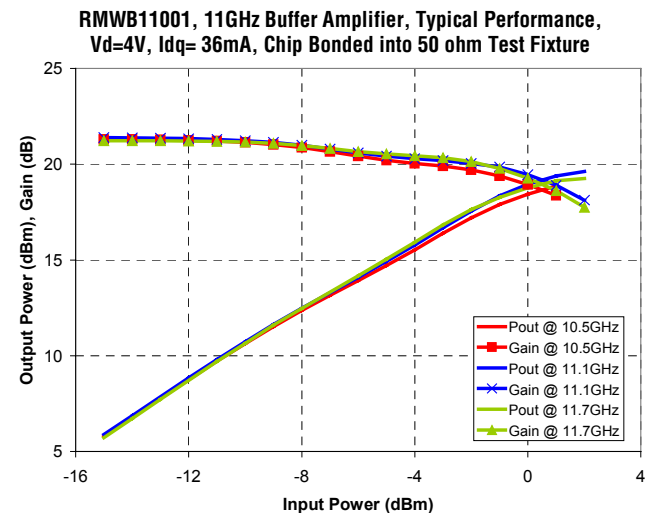
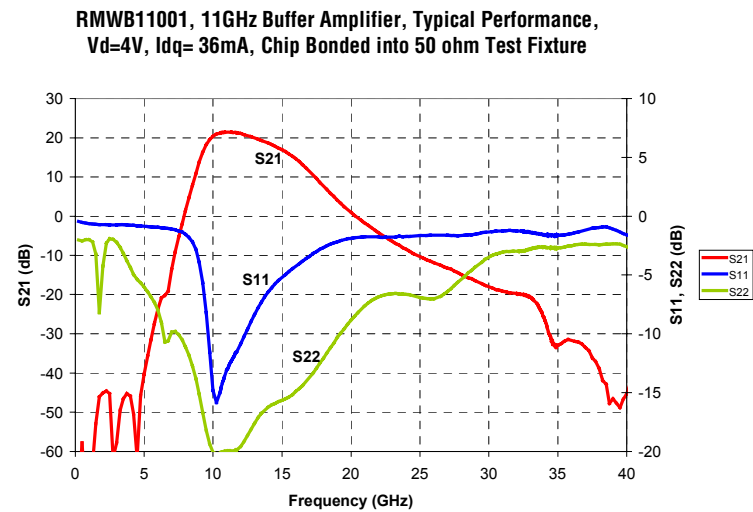
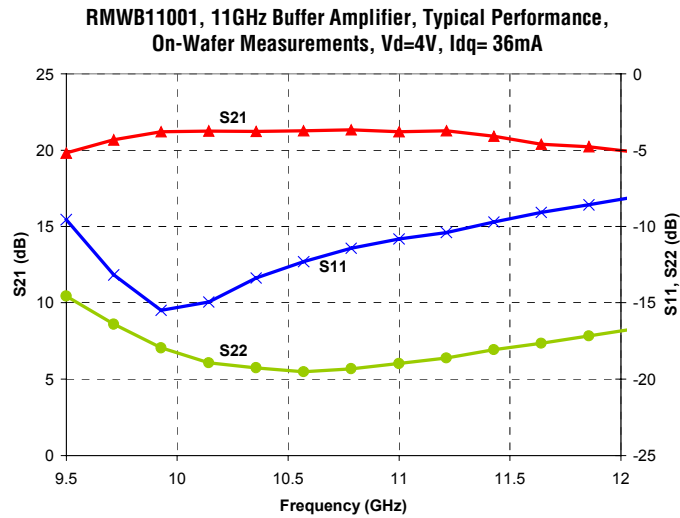
- (i) Turn off RF input power,
- (ii) Turn down and off drain voltage (Vd),
- (iii) Turn down and off gate bias voltage (Vg).

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Performance Data



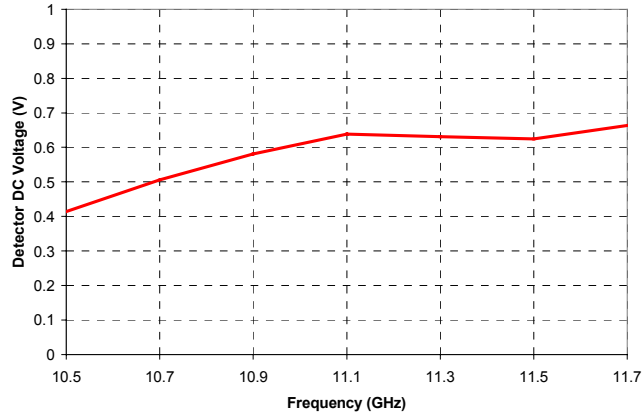
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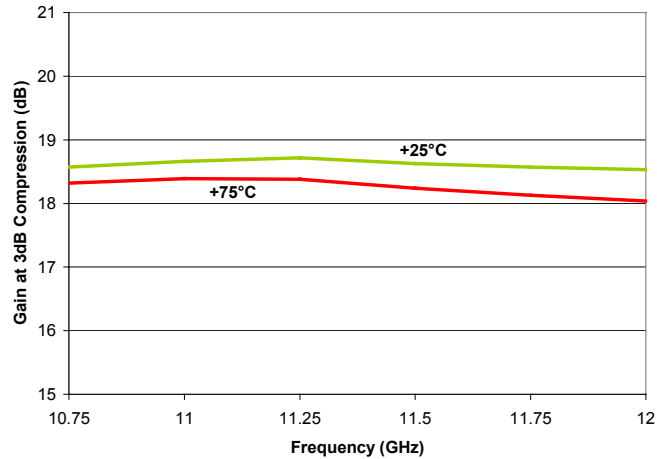
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Performance Data

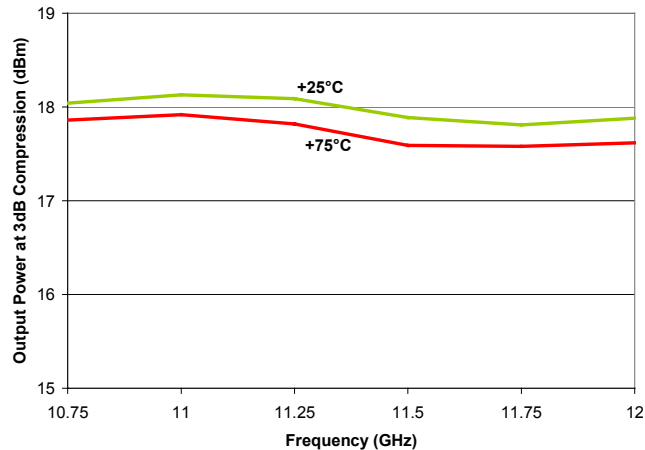
RMWB11001, 11GHz Buffer Amplifier, Typical Performance, Vd=4V, Idq= 36mA, Detector Voltage into 3k ohm load at Pout=+18dBm



RMWB11001, Typical Performance Variation with Temperature, Vd=4V, Idq= 36mA, Chip Bonded into 50 ohm Test Fixture



RMWB11001, Typical Performance Variation with Temperature, Vd=4V, Idq= 36mA, Chip Bonded into 50 ohm Test Fixture



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