3.3V, Synchronous 16-Bit to 32-Bit FET Mux/Demux *NanoSwitch*™

Product Features

- Near-Zero propagation delay.
- 5-ohm Switches Connect Between Two Ports
- Packages Available :
  - 56-pin 240mil Wide Thin Plastic TSSOP(A)
  - 56-pin 300mil Wide Plastic SSOP(V)

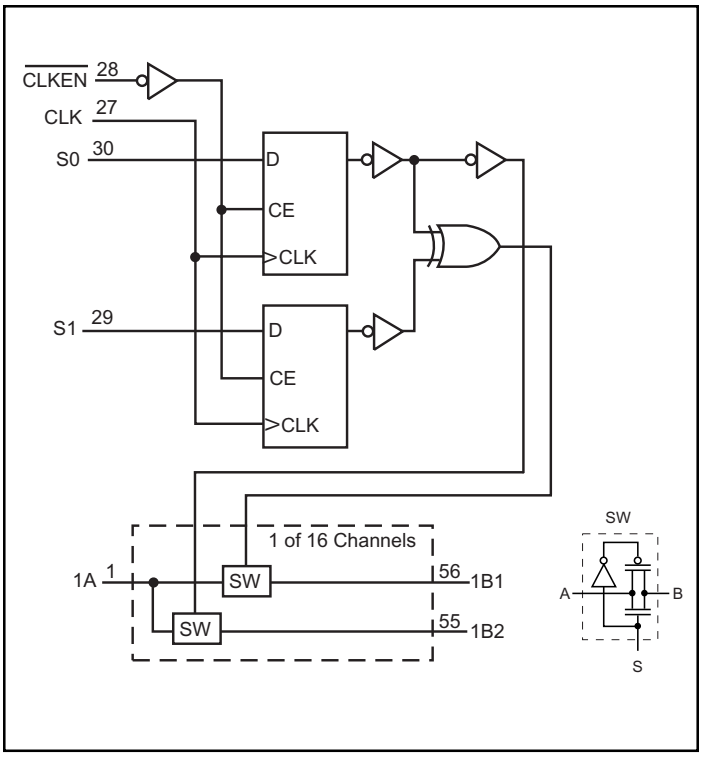
Product Description

Pericom Semiconductor's PI3B series of logic circuits are produced using the company's advanced submicron CMOS technology.

The PI3B16232 is a 3.3 volt, 16-bit to 32-bit synchronous switch.

Two select inputs (S0 and S1) control the data flow. A clock (CLK) and a clock enable ($\overline{CLKEN}$) synchronize the device operation. When $\overline{CLKEN}$ is high, the bus switch remains in the last clocked function.

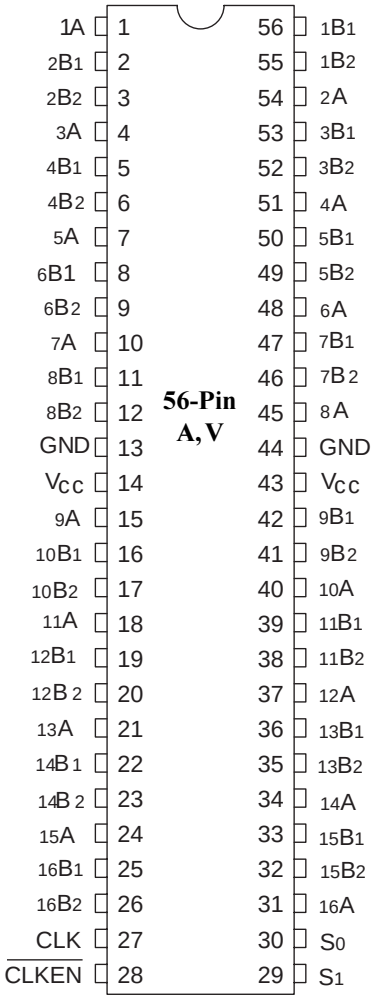
Logic Block Diagram



Truth Table

S1	S0	CLK	$\overline{CLKEN}$	Function
X	X	X	H	Last State
L	L	↑	L	Disconnect
L	H	↑	L	A = B1 and A = B2
H	L	↑	L	A = B1
H	H	↑	L	A = B2

Product Pin Configuration



Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage Range	–0.5V to +4.6V
DC Input Voltage	–0.5V to +4.6V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 3.0V to 3.6V)

Parameters	Description	Test Conditions[1]	Min.	Typ[1]	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0	–	–	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	–0.5	–	0.8	
I_{IH}	Input High Current	V_{CC} = Max., V_{IN} = V_{CC}	–	–	±1	µA
I_{IL}	Input Low Current	V_{CC} = Max., V_{IN} = GND	–	–	±1	
I_{OZH}	High Impedance Output Current	0 ≤ A, B ≤ V_{CC}	–	–	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., V_{IN} = –18MA	–	–0.7	–1.2	V
R_{ON}	Switch ON Resistance[3]	V_{CC} = Min., I_{IN} = 0.0V, I_{ON} = 48mA or 64mA	–	5	8	Ω
		V_{CC} = Min., V_{IN} = 2.4V, I_{ON} = 15mA		10	15	

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[4]	Description	Test Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	3.0	pF
C_{ON}	A/B Capacitance, Switch On		25.0	

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at V_{CC} = 3.3V, T_A = 25°C ambient and maximum loading.
3. Measured by the voltage drop between A and B pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A,B) pins.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions(1)		Min.	Typ(2)	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}			10	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.	V_{IN} = 3.0V(3)			750	
I_{CCD}	Supply Current per Input per MHz(4)	V_{CC} = Max., A & B Pins Open BE = GND Control Input Toggling 50% Duty Cycle				0.25	mA/ MHz

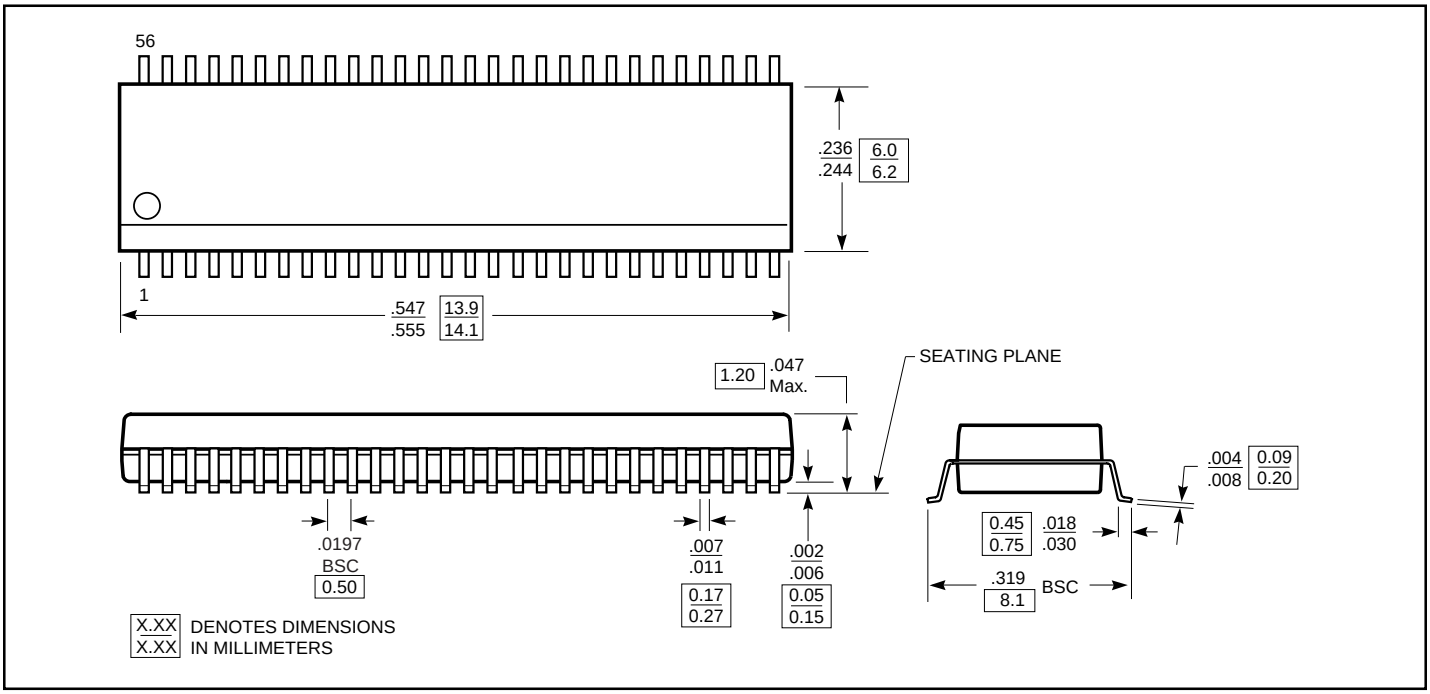
Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for applicable device.
2. Typical values are at Vcc = 3.3V, +25°C ambient.
3. Per TTL driven input (control inputs only); A and B pins do not contribute to Icc.
4. This current applies to the control inputs only and represent the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is not tested, but is guaranteed by design.

Switching Characteristics over Operating Range

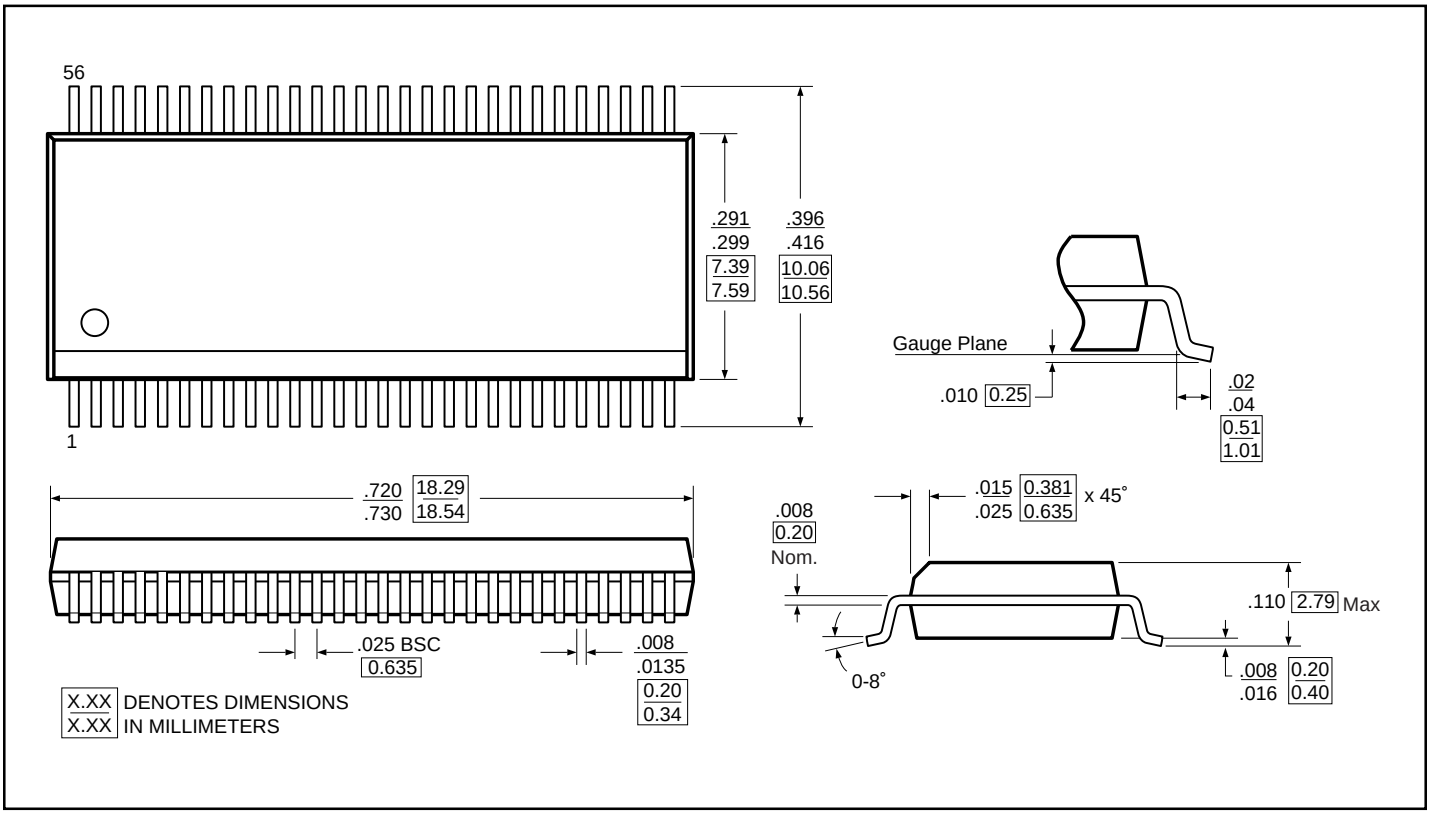
Parameter	Description	Test Conditions(1)	V_{CC} = 3.0 to 3.6V		Units
			Min.	Max.	
f_{CLK}	Clock Frequency		0	150	MHz
tw	Pulse Duration	CLK high or low	3.3		ns
ts	Setup Time	S0, S1 before CLK↑	1.9		
		$\overline{\text{CLKEN}}$ before CLK↑	1.9		
th	Hold Time	S0, S1 after CLK↑	1		
		$\overline{\text{CLKEN}}$ after CLK↑	1.8		
ten	Enable Time	CLK to B1, B2	1	5	
tdis	Disable Time	CLK to B1, B2	1	6	
tpd_1(2,3)	Propagation Delay	A to B		0.25	
tpd_2	Propagation Delay	CLK to A	1	4.5	

Notes:
1. See Test Circuits and Waveforms.
2. This parameter is guaranteed by design but not tested.
3. The bus switch contributes no propagational delay other than the RC delay of ON resistance of the switch and the load capacitance.

56-pin 240mil Wide Thin Plastic TSSOP (A) Package



56-pin 300mil Wide Plastic SSOP (V) Package



Applications Information

Logic Inputs

The logic control inputs can be driven up to +3.6V regardless of the supply voltage. For example, given a + 3.3V supply, IN may be driven low to 0V and high to 3.6V. Driving IN Rail-to-Rail® minimizes power consumption.

Power-Supply Sequencing and Hot-Plug Information

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V_{CC} and GND before applying signals to input/output or control pins.

Rail-to-Rail is a registeredtrademark of Nippon Motorola, Ltd.

Ordering Information

Part	Pin	Package	Width	Temperature
PI3B16222A	56	TSSOP	240-mil	–40°C to 85°C
PI3B16222V		SSOP	300-mil	