

# MC74VHCT32A

## Quad 2-Input OR Gate / CMOS Logic Level Shifter with LSTTL – Compatible Inputs

The MC74VHCT32A is an advanced high speed CMOS 2-input OR gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device input is compatible with TTL-type input thresholds and the output has a full 5.0 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic-level translator from 3.0 V CMOS logic to 5.0 V CMOS Logic or from 1.8 V CMOS logic to 3.0 V CMOS Logic while operating at the high-voltage power supply.

The MC74VHCT32A input structure provides protection when voltages up to 7.0 V are applied, regardless of the supply voltage. This allows the MC74VHCT32A to be used to interface 5.0 V circuits to 3.0 V circuits. The output structures also provide protection when  $V_{CC} = 0$  V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

### Features

- High Speed:  $t_{PD} = 3.8$  ns (Typ) at  $V_{CC} = 5.0$  V
- Low Power Dissipation:  $I_{CC} = 2$   $\mu$ A (Max) at  $T_A = 25^\circ$ C
- TTL-Compatible Inputs:  $V_{IL} = 0.8$  V;  $V_{IH} = 2.0$  V
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise:  $V_{OLP} = 0.8$  V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
  - Human Body Model > 2000 V;
  - Machine Model > 200 V
- Pb-Free Packages are Available\*

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



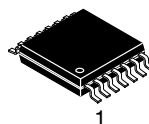
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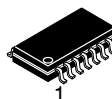
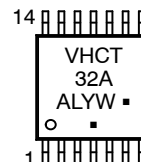
### MARKING DIAGRAMS†



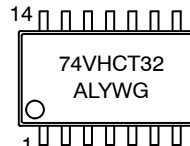
SOIC-14  
D SUFFIX  
CASE 751A



TSSOP-14  
DT SUFFIX  
CASE 948G



SOEIAJ-14  
M SUFFIX  
CASE 965



A = Assembly Location  
WL, L = Wafer Lot  
Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

†For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

# MC74VHCT32A

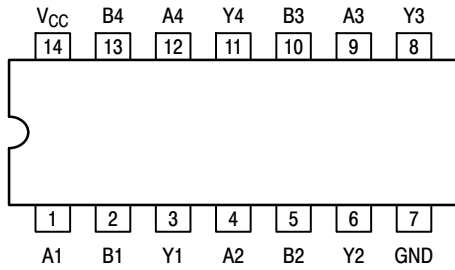


Figure 1. Pin Connection and Marking Diagram (Top View)

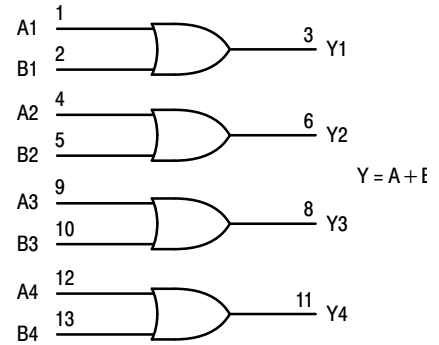


Figure 2. Logic Diagram

Table 1. FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage	-0.5 to +7.0	V
$V_{in}$	DC Input Voltage	-0.5 to +7.0	V
$V_{out}$	DC Output Voltage $V_{CC} = 0$ High or Low State	-0.5 to +7.0 -0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	Input Diode Current	-20	mA
$I_{OK}$	Output Diode Current ( $V_{OUT} < GND$ ; $V_{OUT} > V_{CC}$ )	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

†Derating - SOIC Packages: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

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## RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	2.0	5.5	V
V <sub>IN</sub>	DC Input Voltage	0.0	5.5	V
V <sub>OUT</sub>	DC Output Voltage V <sub>CC</sub> = 0 High or Low State	0.0 0.0	5.5 V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature Range	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time V <sub>CC</sub> = 3.3V ± 0.3V V <sub>CC</sub> = 5.0V ± 0.5V	0 0	100 20	ns/V

## NOISE CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0 ns, C<sub>L</sub> = 50 pF, V<sub>CC</sub> = 5.0 V)

Symbol	Characteristic	T <sub>A</sub> = 25°C		Unit
		Typ	Max	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	0.3	0.8	V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	-0.3	-0.8	V
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage		3.5	V
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage		1.5	V

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			T <sub>A</sub> ≤ 85°C		T <sub>A</sub> ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V <sub>IH</sub>	Minimum High-Level Input Voltage		3.0	1.2			1.2		1.2		V
			4.5	2.0			2.0		2.0		
			5.5	2.0			2.0		2.0		
V <sub>IL</sub>	Maximum Low-Level Input Voltage		3.0			0.53		0.53		0.53	V
			4.5			0.8		0.8		0.8	
			5.5			0.8		0.8		0.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -50 μA	3.0	2.9	3.0		2.9		2.9		V
			4.5	4.4	4.5		4.4		4.4		
V <sub>OL</sub>	Maximum Low-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -4 mA I <sub>OH</sub> = -8 mA	3.0	2.58			2.48		2.34		V
			4.5	3.94			3.80		3.66		
V <sub>OL</sub>	Maximum Low-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 50 μA	3.0		0.0	0.1		0.1		0.1	V
			4.5		0.0	0.1		0.1		0.1	
V <sub>OL</sub>	Maximum Low-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 4 mA I <sub>OL</sub> = 8 mA	3.0			0.36		0.44		0.52	V
			4.5			0.36		0.44		0.52	
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5			2.0		20		40	μA
I <sub>CC</sub> T	Quiescent Supply Current	Input: V <sub>IN</sub> = 3.4 V	5.5			1.35		1.50		1.65	mA
I <sub>OPD</sub>	Output Leakage Current	V <sub>OUT</sub> = 5.5 V	0.0			0.5		5.0		10	μA

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## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = -40$ to $125^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, A or B to Y	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF $C_L = 50$ pF		5.5 8.0	7.9 11.4	1.0 1.0	9.5 13.0	ns
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $C_L = 50$ pF		3.8 5.3	5.5 7.5	1.0 1.0	6.5 8.5	
$C_{in}$	Maximum Input Capacitance			4 10			10	pF

$C_{PD}$	Power Dissipation Capacitance (Note 1)	Typical @ $25^\circ\text{C}$ , $V_{CC} = 5.0\text{V}$		pF
		22		
				pF

1.  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/4$  (per gate).  $C_{PD}$  is used to determine the no-load dynamic power consumption;  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$ .

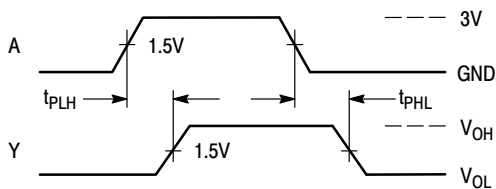
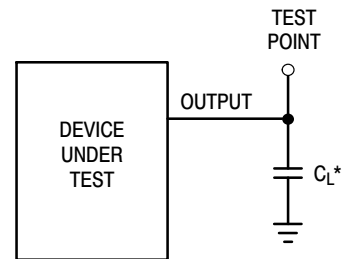


Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance

Figure 2. Test Circuit

## ORDERING INFORMATION

Device	Package	Shipping†
MC74VHCT32ADR2	SOIC-14	2500 / Tape & Reel
MC74VHCT32ADR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
MC74VHCT32ADTR2	TSSOP-14*	2500 / Tape & Reel
MC74VHCT32ADTR2G	TSSOP-14*	2500 / Tape & Reel
MC74VHCT32AM	SOEIAJ-14	50 Units / Rail
MC74VHCT32AMG	SOEIAJ-14 (Pb-Free)	50 Units / Rail
MC74VHCT32AMEL	SOEIAJ-14	2000 / Tape & Reel
MC74VHCT32AMELG	SOEIAJ-14 (Pb-Free)	2000 / Tape & Reel

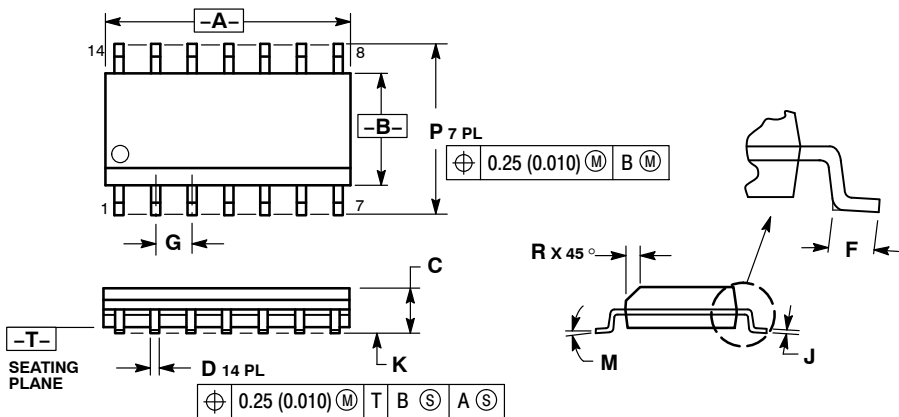
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

# MC74VHCT32A

## PACKAGE DIMENSIONS

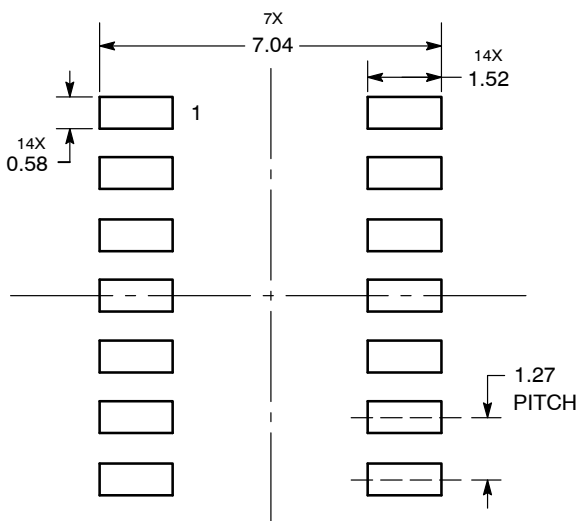
SOIC-14  
CASE 751A-03  
ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

## SOLDERING FOOTPRINT



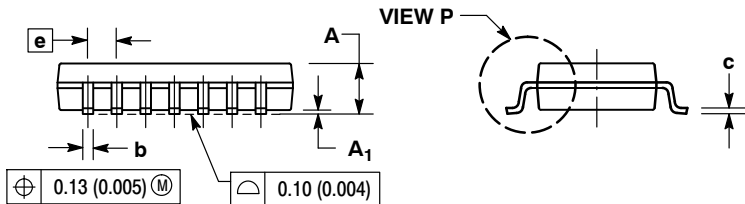
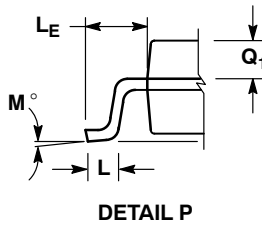
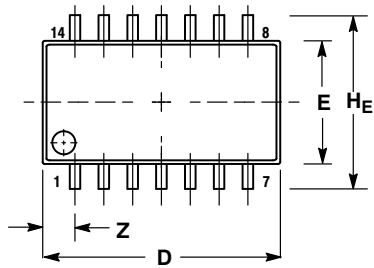
DIMENSIONS: MILLIMETERS



# MC74VHCT32A

## PACKAGE DIMENSIONS

SOEIAJ-14  
M SUFFIX  
CASE 965-01  
ISSUE B



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H <sub>E</sub>	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L <sub>E</sub>	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

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