Triple 2-3-2-Input OR/NOR Gate

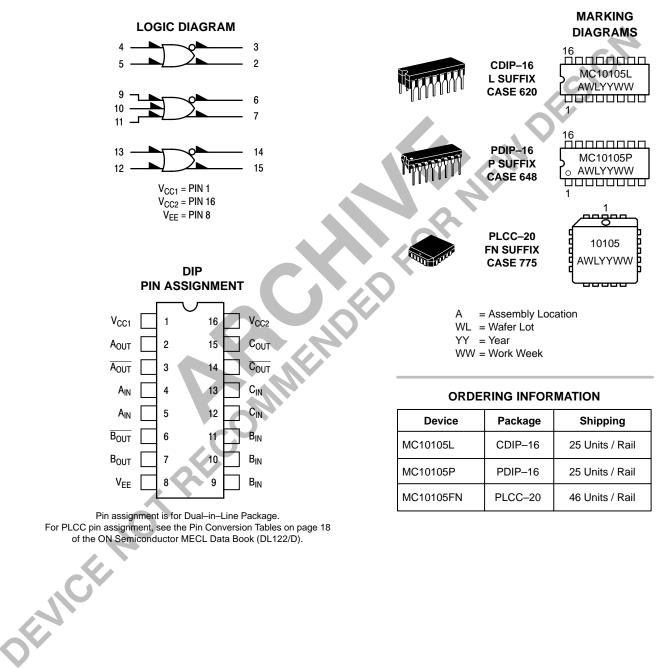
The MC10105 is a triple 2–3–2 input OR/NOR gate.

- $P_D = 30 \text{ mW typ/gate (No Load)}$
- $t_{pd} = 2.0 \text{ ns typ}$
- t_r , $t_f = 2.0$ ns typ (20%-80%)



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ELECTRICAL CHARACTERISTICS

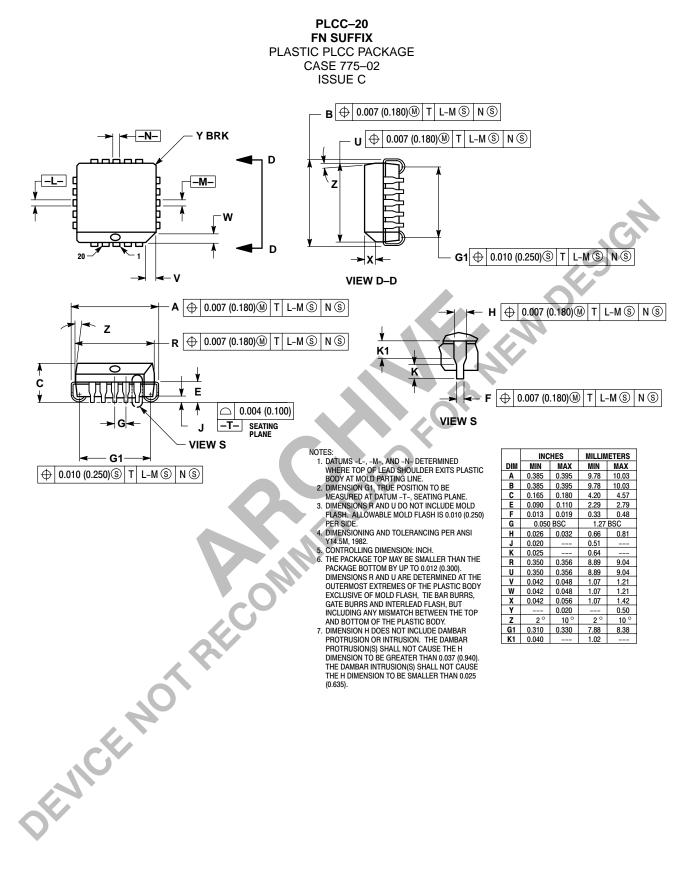
| $ \begin{array}{ c c c c c c c c c c c c c c c c c c c$ | Characteristic | | D ¹ | Test Limits | | | | - | | | |
|--|------------------------------------|--|-----------------------|-------------------|------------|------------|------------|------------|------------|------------------|-----|
| $\begin{array}{ c c c c c c c c c c c c c c c c c c c$ | Characteristic | | Pin Under | -30°C +25°C +85°C | | | | | 5°C | | |
| $\begin{array}{ c c c c c c c c c c c c c c c c c c c$ | | Symbol | | Min | Max | Min | Тур | Max | Min | Max | Un |
| $\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$ | Power Supply Drain Current | ١ _E | 8 | | 23 | | 17 | 21 | | 23 | mAc |
| $\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$ | Input Current | I _{inH} | 4 | | 425 | | | 265 | | 265 | μAd |
| $\begin{array}{ c c c c c c c c c c c c c c c c c c c$ | | | 4 | 0.5 | | 0.5 | | | 0.3 | | μAd |
| $\begin{array}{ c c c c c c c c c c c c c c c c c c c$ | Output Voltage Logic 1 | | | | | | | | | | Vdo |
| $\begin{array}{ c c c c c c c c c c c c c c c c c c c$ | Output Voltage Logic 0 | V _{OL} | | | | | | | | | Vde |
| $\begin{array}{c c c c c c c c c c c c c c c c c c c $ | Threshold Voltage Logic 1 | V _{OHA} | | | | | | | | | Vd |
| $\begin{array}{c ccccccccccccccccccccccccccccccccccc$ | Threshold Voltage Logic 0 | V _{OLA} | | | | | | | | -1.595 -1.595 | Vdo |
| table <th< td=""><td>Switching Times (50Ω Load)</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>ns</td></th<> | Switching Times (50 Ω Load) | | | | | | | | | | ns |
| t2+ 2 1.1 3.6 1.1 2.0 3.3 1.1 3.7 Fall Time (20 to 80%) t_{3-} 3 1.1 3.6 1.1 2.0 3.3 1.1 3.7 L t_{2-} 2 1.1 3.6 1.1 2.0 3.3 1.1 3.7 L t_{2-} 2 1.1 3.6 1.1 2.0 3.3 1.1 3.7 | Propagation Delay | t _{4–3+} t ₄₊₂₊ | 3 2 | 1.0 1.0 | 3.1 3.1 | 1.0 1.0 | 2.0 2.0 | 2.9 2.9 | 1.0 1.0 | 3.3 3.3 | |
| t ₂ 2 1.1 3.6 1.1 2.0 3.3 1.1 3.7 | Rise Time (20 to 80%) | | | | | | | | | | |
| | Fall Time (20 to 80%) | | | | | | | | | | |
| | | 5 | 2 | | ND | | | | | | |
| | of Mot N | | | | | | | | | | |

ELECTRICAL CHARACTERISTICS (continued)

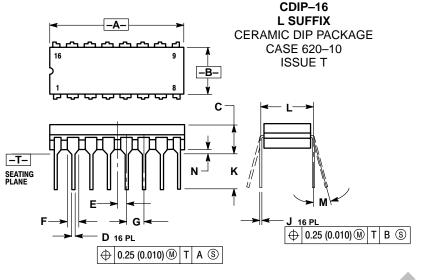
| | | | | | TAGE VALU | GE VALUES (Volts) | | | |
|--------------------|--------------------|--|------------------|--------------------|---|---------------------|---------------------|------------------|---|
| | | @ Test Te | mperature | V _{IHmax} | V _{ILmin} | V _{IHAmin} | V _{ILAmax} | V _{EE} | |
| | | | –30°C | -0.890 | -1.890 | -1.205 | -1.500 | -5.2 | |
| | | | +25°C | -0.810 | -1.850 | -1.105 | -1.475 | -5.2 | |
| | | | +85°C | -0.700 | -1.825 | -1.035 | -1.440 | -5.2 | |
| | | | Pin | TEST V | TEST VOLTAGE APPLIED TO PINS LISTED BELOW | | | | |
| Character | istic | Symbol | Under Test | V _{IHmax} | V _{ILmin} | V _{IHAmin} | V _{ILAmax} | V _{EE} | (V _{CC}) Gnd |
| Power Supply Drain | Current | Ι _Ε | 8 | | | | | 8 | 1, 16 |
| Input Current | | l _{inH} | 4 | 4 | | | | 8 | 1, 16 |
| | | I _{inL} | 4 | | 4 | | | 8 | 1, 16 |
| Output Voltage | Logic 1 | V _{OH} | 3 2 | 4 | | | | 8 8 | 1, 16 1, 16 |
| Output Voltage | Logic 0 | V _{OL} | 3 2 | 4 | | | | 8 8 | 1, 16 1, 16 |
| Threshold Voltage | Logic 1 | V _{OHA} | 3 2 | | | 4 | 4 | 8 8 | 1, 16 1, 16 |
| Threshold Voltage | Logic 0 | V _{OLA} | 3 2 | | | 4 | 4 | 8 8 | 1, 16 1, 16 |
| Switching Times | (50 Ω Load) | | | | | Pulse In | Pulse Out | –3.2 V | +2.0 V |
| Propagation Delay | | t ₄₊₃₋ t ₄₋₃₊ t ₄₊₂₊ t ₄₋₂₋ | 3 3 2 2 | | | 4 4 4 4 | 3 3 2 2 | 8 8 8 8 | 1, 16 1, 16 1, 16 1, 16 1, 16 |
| Rise Time | (20 to 80%) | t ₃₊ t ₂₊ | 3 2 | | | 4 4 | 3 2 | 8 8 | 1, 16 1, 16 |
| Fall Time | (20 to 80%) | t ₃₋ t ₂₋ | 3 2 | | | 4 4 | 3 2 | 8 8 | 1, 16 1, 16 |

te terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the area manner.

PACKAGE DIMENSIONS



PACKAGE DIMENSIONS



NOTES:

DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
CONTROLLING DIMENSION: INCH.
DIMENSION L TO CENTER OF LEAD WHEN FOOMED DRAWLES

DIMENSION F TO CENTER OF LEAD WHEN FORMED PARALLEL.
DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

| | INC | HES | MILLIMETERS | | |
|-----|-----------|-------|-------------|-------|--|
| DIM | MIN MAX | | MIN MAX | | |
| Α | 0.750 | 0.785 | 19.05 | 19.93 | |
| В | 0.240 | 0.295 | 6.10 | 7.49 | |
| С | | 0.200 | | 5.08 | |
| D | 0.015 | 0.020 | 0.39 | 0.50 | |
| Е | 0.050 BSC | | 1.27 BSC | | |
| F | 0.055 | 0.065 | 1.40 | 1.65 | |
| G | 0.100 BSC | | 2.54 | BSC | |
| Н | 0.008 | 0.015 | 0.21 | 0.38 | |
| Κ | 0.125 | 0.170 | 3.18 | 4.31 | |
| L | 0.300 BSC | | 7.62 BSC | | |
| М | 0° 15° | | 0 ° | 15° | |
| Ν | 0.020 | 0.040 | 0.51 | 1.01 | |

-A-<u>ሳ ስ ስ ስ</u> 16 В 0 L $\Box \Box$ ι, հո - C S -T- SEATING PLANE H G **D** 16 PL

PDIP-16 **P SUFFIX** PLASTIC DIP PACKAGE CASE 648-08 ISSUE R

NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH. 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL. 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH. 5. ROUNDED CORNERS OPTIONAL.

| Ĭ | | INC | HES | MILLIMETERS | | |
|---|-----|-------|-------|-------------|--------------|--|
| | DIM | MIN | MAX | MIN | MAX 19.55 | |
| ļ | DIN | IVIIN | IVIAA | IVIIIN | | |
| | Α | 0.740 | 0.770 | 18.80 | | |
| | В | 0.250 | 0.270 | 6.35 | 6.85 | |
| | С | 0.145 | 0.175 | 3.69 | 4.44 | |
| | D | 0.015 | 0.021 | 0.39 | 0.53 | |
| [| F | 0.040 | 0.70 | 1.02 | 1.77 | |
| | G | 0.100 | BSC | 2.54 | BSC | |
| | Н | 0.050 | BSC | 1.27 BSC | | |
| | J | 0.008 | 0.015 | 0.21 | 0.38 | |
| [| Κ | 0.110 | 0.130 | 2.80 | 3.30 | |
| [| L | 0.295 | 0.305 | 7.50 | 7.74 | |
| | М | 0° | 10 ° | 0 ° | 10 ° | |
| | S | 0.020 | 0.040 | 0.51 | 1.01 | |

Notes

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Notes

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