

# 1. General description

The 74LVC32A provides four 2-input OR gates.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V applications.

# 2. Features and benefits

- 5 V tolerant inputs for interlacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard:
  - ◆ JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

# 3. Ordering information

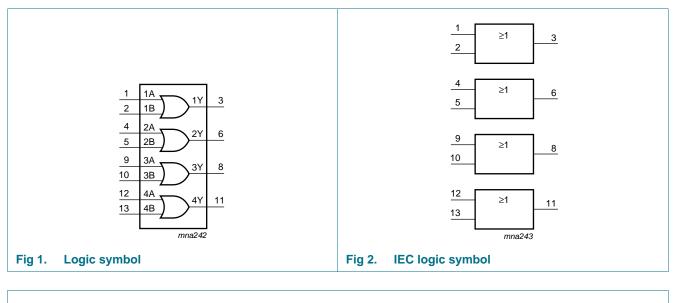
#### Table 1.Ordering information

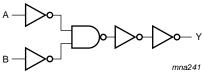
Type number	Package						
	Temperature range Name		Description	Version			
74LVC32AD	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1			
74LVC32ADB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1			
74LVC32APW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1			
74LVC32ABQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85$ mm	SOT762-1			



74LVC32A **Quad 2-input OR gate** 

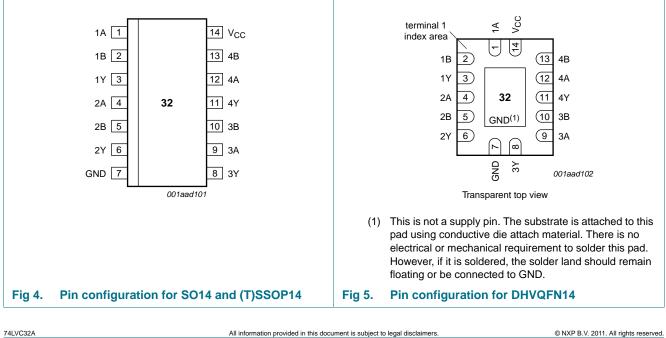
#### **Functional diagram** 4.





Logic diagram for one gate Fig 3.

#### **Pinning information** 5.



# 5.1 Pinning

# 5.2 Pin description

Table 2. Pin de	scription	
Symbol	Pin	Description
1A, 2A, 3A, 4A	1, 4, 9, 12	data input
1B, 2B, 3B, 4B	2, 5, 10, 13	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

# 6. Functional description

Table 3. Function selection <sup>[1]</sup>
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Input		Output
nA	nB	nY
L	L	L
Х	Н	Н
н	Х	Н

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care

# 7. Limiting values

### Table 4.Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

					,
Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V
I <sub>IK</sub>	input clamping current	V <sub>1</sub> < 0	-50	-	mA
VI	input voltage		<u>[1]</u> –0.5	+6.5	V
I <sub>OK</sub>	output clamping current	$V_{\rm O} > V_{\rm CC}$ or $V_{\rm O} < 0$	-	±50	mA
Vo	output voltage		<u>[2]</u> –0.5	$V_{CC} + 0.5$	V
lo	output current	$V_{O} = 0 V$ to $V_{CC}$	-	±50	mA
I <sub>CC</sub>	supply current		-	100	mA
I <sub>GND</sub>	ground current		-100	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	$T_{amb} = -40 \ ^{\circ}C \ to +125 \ ^{\circ}C$	[3] _	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

For SO14 packages: above 70 °C derate linearly with 8 mW/K.
 For (T)SSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.
 For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

# 8. Recommended operating conditions

Table 5.	Recommended operating con	ditions				
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CC</sub>	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	-	+125	°C
$\Delta t / \Delta V$	input transition rise and fall rate	$V_{CC}$ = 1.65 V to 2.7 V	0	-	20	ns/V
		$V_{CC}$ = 2.7 V to 3.6 V	0	-	10	ns/V

# 9. Static characteristics

### Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			-40 °C to	Unit	
			Min	Typ <mark>[1]</mark>	Мах	Min	Max	-
VIH	HIGH-level	V <sub>CC</sub> = 1.2 V	1.08	-	-	1.08	-	V
	input voltage	$V_{CC}$ = 1.65 V to 1.95 V	$0.65 \times V_{CC}$	-	-	$0.65 \times V_{CC}$	-	V
		$V_{CC}$ = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		$V_{CC}$ = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
VIL	LOW-level	V <sub>CC</sub> = 1.2 V	-	-	0.12	-	0.12	V
	input voltage	$V_{CC}$ = 1.65 V to 1.95 V	-	-	$0.35 \times V_{CC}$	-	$0.35 \times V_{CC}$	V
		$V_{CC}$ = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		$V_{CC}$ = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level	$V_{I} = V_{IH} \text{ or } V_{IL}$						
	output voltage	$I_{O} = -100 \ \mu A;$ $V_{CC} = 1.65 \ V \text{ to } 3.6 \ V$	$V_{CC}-0.2$	-	-	$V_{CC}-0.3$	-	V
		$I_{O} = -4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.2	-	-	1.05	-	V
		$I_{O}$ = -8 mA; $V_{CC}$ = 2.3 V	1.8	-	-	1.65	-	V
		$I_0 = -12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	2.2	-	-	2.05	-	V
		$I_{O} = -18 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.4	-	-	2.25	-	V
		$I_{O} = -24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.2	-	-	2.0	-	V
V <sub>OL</sub>	LOW-level	$V_{I} = V_{IH} \text{ or } V_{IL}$						
	output voltage	$I_{O} = 100 \ \mu A;$ $V_{CC} = 1.65 \ V \text{ to } 3.6 \ V$	-	-	0.2	-	0.3	V
		$I_0 = 4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.45	-	0.65	V
		$I_0 = 8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.6	-	0.8	V
		$I_0$ = 12 mA; $V_{CC}$ = 2.7 V	-	-	0.4	-	0.6	V
		$I_0 = 24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.55	-	0.8	V
I	input leakage current	$V_{CC}$ = 3.6 V; $V_{I}$ = 5.5 V or GND	-	±0.1	±5	-	±20	μΑ

**Quad 2-input OR gate** 

Symbol Parameter	Parameter	Conditions	-4	) °C to +8	35 °C	–40 °C t	–40 °C to +125 °C		
			Min	Typ <mark>[1]</mark>	Max	Min	Max		
I <sub>CC</sub>	supply current	$V_{CC} = 3.6 \text{ V}; V_I = V_{CC} \text{ or GND};$ $I_O = 0 \text{ A}$	-	0.1	10	-	40	μA	
ΔI <sub>CC</sub>	additional supply current	per input pin; $V_{CC} = 2.7 V$ to 3.6 V; $V_I = V_{CC} - 0.6 V$ ; $I_O = 0 A$	-	5	500	-	5000	μA	
CI	input capacitance	$V_{CC} = 0 V$ to 3.6 V; $V_{I} = GND$ to $V_{CC}$	-	4.0	-	-	-	pF	

#### Table 6. Static characteristics ... continued

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.

# **10. Dynamic characteristics**

#### Table 7. **Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 7.

Symbol	Parameter	Conditions		–40 °C to +85 °C		–40 °C to +125 °C		Unit	
				Min	Typ[1]	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nA, nB to nY; see Figure 6	[2]						
		V <sub>CC</sub> = 1.2 V		-	10	-	-	-	ns
		$V_{CC}$ = 1.65 V to 1.95 V		0.5	4.2	9.0	0.5	10.4	ns
		$V_{CC}$ = 2.3 V to 2.7 V		1.5	2.4	4.9	1.05	5.7	ns
		$V_{CC} = 2.7 V$		1.5	2.5	4.4	1.5	5.5	ns
		$V_{CC}$ = 3.0 V to 3.6 V		1.0	2.2	3.8	1.0	5.0	ns
t <sub>sk(o)</sub>	output skew time	$V_{CC} = 3.0 \text{ V} \text{ to } 3.6 \text{ V}$	[3]	-	-	1.0	-	1.5	ns
C <sub>PD</sub>	power dissipation	per gate; $V_I$ = GND to $V_{CC}$	[4]						
	capacitance	$V_{CC}$ = 1.65 V to 1.95 V		-	4.7	-	-	-	pF
		$V_{CC}$ = 2.3 V to 2.7 V		-	8.0	-	-	-	pF
		$V_{CC}$ = 3.0 V to 3.6 V		-	11.0	-	-	-	pF

[1] Typical values are measured at  $T_{amb}$  = 25 °C and  $V_{CC}$  = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

- [2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .
- [3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:

 $f_i$  = input frequency in MHz;  $f_o$  = output frequency in MHz

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in Volts

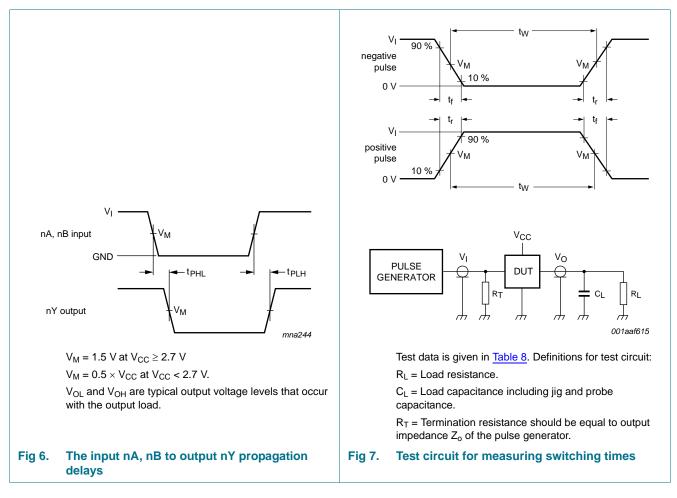
N = number of inputs switching

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs

74LVC32A

Quad 2-input OR gate

# 11. AC waveforms

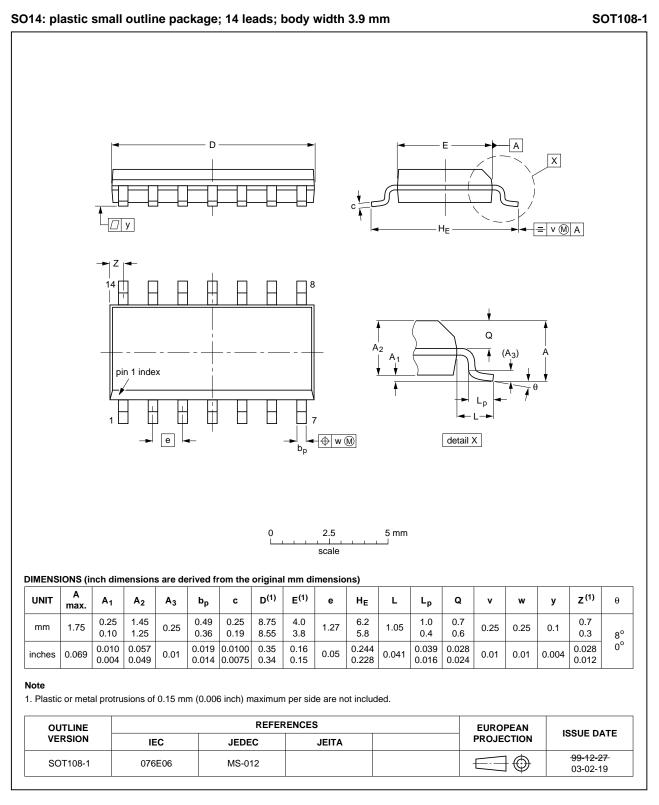


#### Table 8. Test data

Supply voltage	Input	Input		
	VI	t <sub>r</sub> , t <sub>f</sub>	CL	RL
1.2 V	V <sub>CC</sub>	$\leq$ 2 ns	30 pF	1 kΩ
1.65 V to 1.95 V	V <sub>CC</sub>	$\leq$ 2 ns	30 pF	1 kΩ
2.3 V to 2.7 V	V <sub>CC</sub>	$\leq$ 2 ns	30 pF	500 Ω
2.7 V	2.7 V	$\leq$ 2.5 ns	50 pF	500 Ω
3.0 V to 3.6 V	2.7 V	$\leq$ 2.5 ns	50 pF	500 Ω

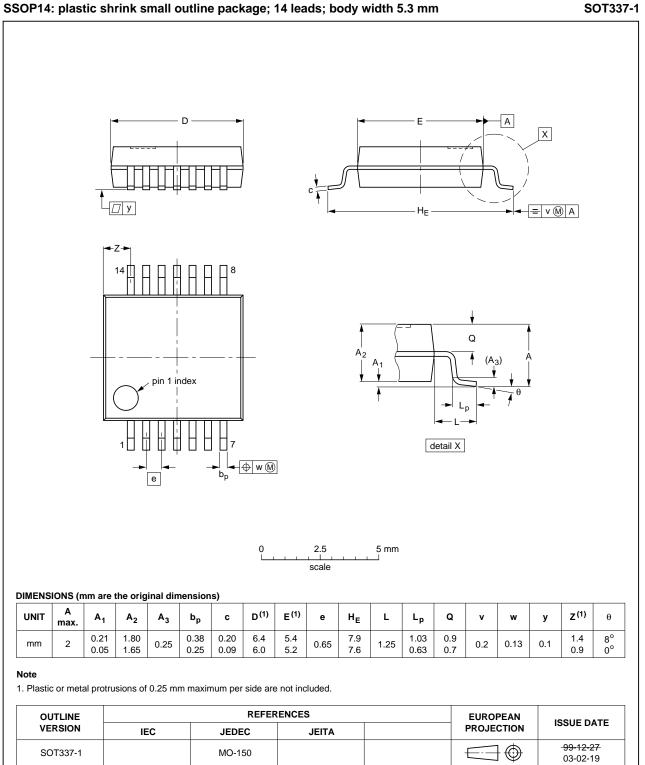
74LVC32A Quad 2-input OR gate

# 12. Package outline



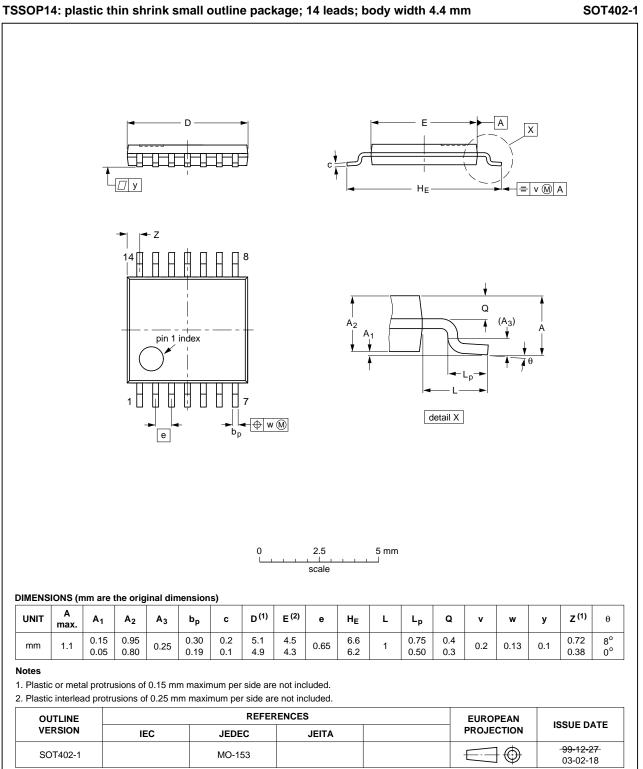
### Fig 8. Package outline SOT108-1 (SO14)

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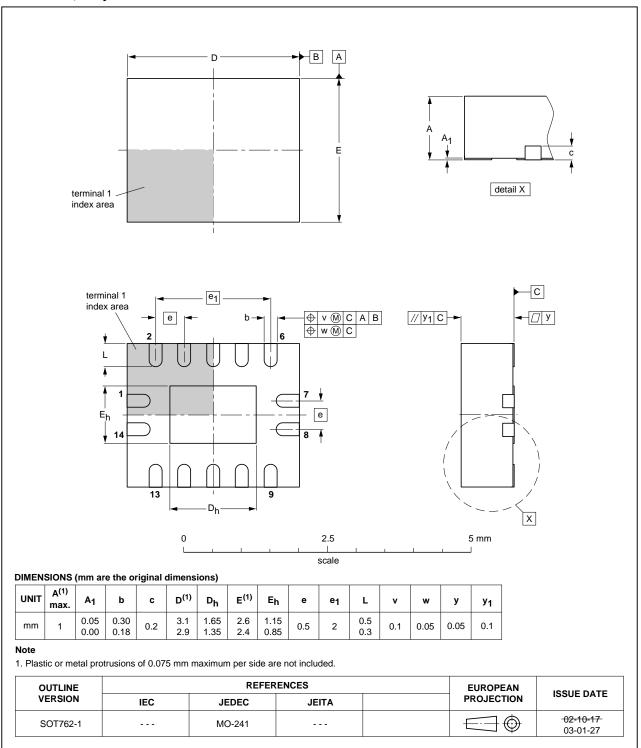
#### Fig 9. Package outline SOT337-1 (SSOP14)

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# Fig 10. Package outline SOT402-1 (TSSOP14)

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#### DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm SOT762-1

### Fig 11. Package outline SOT762-1 (DHVQFN14)

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# **13. Abbreviations**

Table 9.	Abbreviations
Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
MM	Machine Model
HBM	Human Body Model
TTL	Transistor-Transistor Logic

# 14. Revision history

Table 10. Re	vision history			
Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC32A v.5	20111117	Product data sheet	-	74LVC32A v.4
Modifications:	<ul> <li>Legal pages upo</li> </ul>	dated.		
	<ul> <li><u>Table 6</u>, bodyrov</li> </ul>	w $\Delta I_{CC}$ : condition $V_{CC}$ changed	ged.	
74LVC32A v.4	20111019	Product data sheet	-	74LVC32A v.3
74LVC32A v.3	20030716	Product specification	-	74LVC32A v.2
74LVC32A v.2	19970630	Product specification	-	74LVC32A v.1
74LVC32A v.1	19970630	Product specification	-	-

# 15. Legal information

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Document status[1][2]	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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# 74LVC32A

# **17. Contents**

1	General description 1
2	Features and benefits 1
3	Ordering information 1
4	Functional diagram 2
5	Pinning information 2
5.1	Pinning 2
5.2	Pin description 3
6	Functional description 3
7	Limiting values 3
8	Recommended operating conditions 4
9	Static characteristics 4
10	Dynamic characteristics 5
11	AC waveforms 6
12	Package outline 7
13	Abbreviations 11
14	Revision history 11
15	Legal information 12
15.1	Data sheet status 12
15.2	Definitions 12
15.3	Disclaimers 12
15.4	Trademarks 13
16	Contact information 13
17	Contents 14

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