MAS9118

Buzzer DAC Interface

This is preliminary information on a new product under development. Micro Analog Systems Oy reserves the right to make any changes without notice.

Preliminary

- **Excellent Frequency Response**
- **High Efficiency 8 Ohms Driver**
- **Serial Interface**
- **Separate Voltages at Interface and Driver**

DESCRIPTION

MAS9118 is a high performance analog interface for buzzer or small loudspeaker. It employs new circuit structures, which provide a possibility to play high quality speech or music by using low cost buzzer or miniature speaker. The driver has excellent power efficiency due to class-D operation and provides high sound pressure due to balanced outputs. The interface is used as any eight bit DAC, just by loading the signal to the input register at regular time intervals.

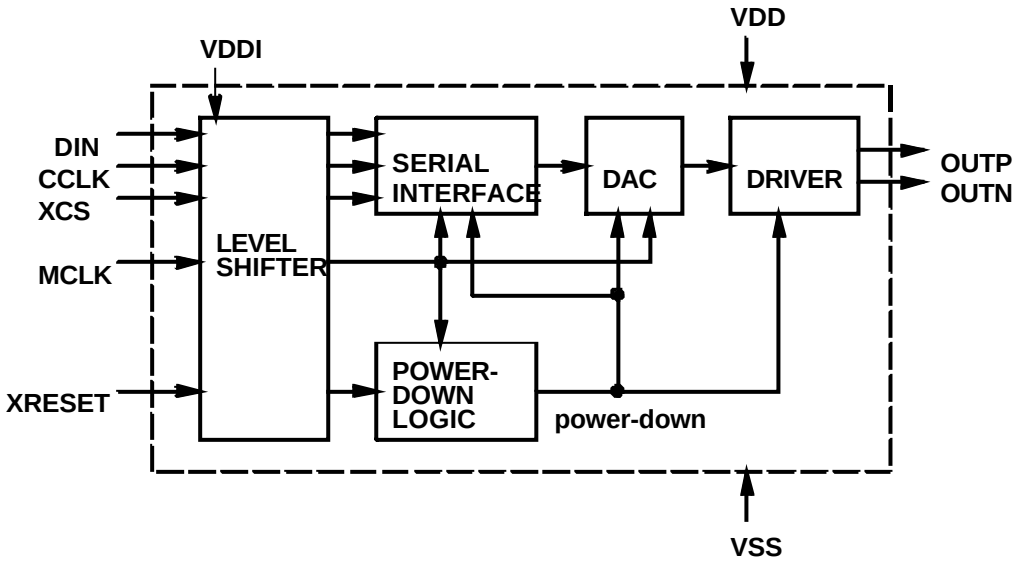
FEATURES

- Excellent Frequency Response
- MSOP Package
- No External Components
- Easy to Use

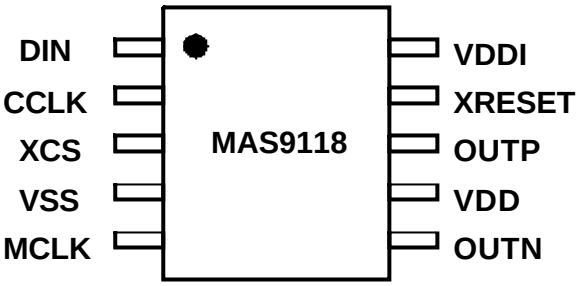
APPLICATION

- Cellular Phones
- Toys

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	Pin	Type	Function
DIN	1	DI	Data Input of the Serial Interface
CCLK	2	DI	Clock Input of the Serial Interface
XCS	3	DI	Chip Select of the Serial Interface, sets the data sampling frequency
VSS	4	P	Ground
MCLK	5	DI	Master Clock Input
OUTN	6	AO	Negative Output for the Buzzer
VDD	7	P	Positive Power Supply
OUTP	8	AO	Positive Output for the Buzzer
XRESET	9	DI	Reset and Power-down, Active Low
VDDI	10	AI	Input Signal High Reference Voltage

GENERAL DESCRIPTION

Main features

The data path of MAS9118 consists of level shifters, serial interface, interpolating digital to analog converter (DAC) and balanced output driver (H-bridge).

MAS9118 produces PWM (pulse width modulated) output signal according to the digital input data sourced through DIN. Because of the PWM output (class-D amplifier) there is no need for external capacitors between MAS9118 output and load element (no DC voltage at output).

The amplifier has excellent power efficiency due to class-D operation. The driver distortion characteristic is load insensitive.

The buzzer is driven in an H-bridge. The driver balanced outputs double the voltage, which is advantageous for portable devices with low voltage.

The device enters to a power-down mode after power-on reset or when XRESET pin is low or when master clock is stopped. Even though the device is internally reset at start-up it is recommended to keep XRESET low when switching powers on and rise XRESET signal up later (a few ms after powers are switched on). Output pins (OUTP, OUTN) are connected to ground voltage (VSS) at power-down mode to prevent some times harmful DC bias at output.

Interfaces

There are level shifters in the input (MCLK, CCLK, DIN, XCS). Input level shifting provides the possibility to use lower signal levels for device control and higher signal level for buzzer driver, which enables higher voltage to buzzer. The operating voltage of the driving circuit should be connected to VDDI, which is a reference level for control signals.

The input signal is written into the internal register via the asynchronous serial interface. Serial interface consists of an input pin for data (DIN), chip select pin (XCS) and control clock (CCLK).

CCLK has to be pulsed eight times while XCS is low to shift the data in. The data is shifted into the serial input register when 8 CCLK pulses has occurred after XCS falling edge. When the eighth rising edge comes the data is re-synchronized with MCLK and passed to the DAC. XCS has to be set high before next data can be read in (data read is started by XCS falling edge). Input data read is cancelled if XCS is set high before all 8 data bits has been read in, and old data remains to device output.

The serial data word length is 8 bits and it is 2-complement with MSB first. The data (word) rate (XCS falling edge -frequency), which is the device output sampling frequency, should be in the range of 8 to 80 kHz for good audio quality.

The master clock (MCLK) is used for the on-chip sigma-delta modulator, which truncates the 8-bit input signal to 1-bit representation. The MCLK is used as a DAC output sampling frequency. To minimize jitter, MCLK should be integer multiple of the sampling frequency (XCS frequency).

Since CCLK and MCLK are allowed to be asynchronous, double buffering for input data is used to guarantee correct operation in all conditions.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min	Max	Unit
Positive Supply	VDD, VDDI			6.0	V
Negative Supply	VSS			-0.3	V
Voltage at Any Digital Input				VSS-1 to VCC+1	V
Storage Temperature			-65	+150	^{o}C
ESD Protection				2000	V
Latch-up Current				±100	mA

Note: Short circuit connection between OUTP/OUTN pins may destroy the device.

RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Positive Supply	VDD		2.5	3.6	5.5	V
Voltage of the Input Signal	VDDI		1.5	1.8	VDD	V
Ambient Temperature	Ta		-40		+85	^{o}C
Standby Current	Istby	no load, zero input		1.0	5.0	mA
Active Current	Idd	8 Ohm load, DIN=1 kHz 0dB sine VDD=2.5V VDD=3.6V VDD=5.5V	 tbd	 86 142 240	 tbd	 mA mA mA
Power Down Leakage Current, Ext. Reset	Ipd1	XRESET=low, MCLK active		21	100	µA
Power Down Leakage Current, Clock Reset	Ipd2	MCLK=low		0.1		µA
Master Clock Frequency	fMCLK		0.5	1	3	MHz

ELECTRICAL CHARACTERISTICS

◆ Analog Characteristics

AC Characteristics

Amplitude Response

(VDD=+3.6V, VDDI=+1.8V, VSS=0V, F_{XCS}=62.5kHz, F_{MCLK}=1000kHz, F_{CCLK}=1000 kHz, Ta=+25 ^{o}C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Absolute Gain Error at 1 kHz	Gabs			0.1		dB
Gain Variation with Frequency	Gaf	Relative to Gabs, f=0…8kHz		0.01		dB
Gain Variation with Signal Level	Gal	Relative to Gabs 0…-12dB		0.5		dB
Gain Variation with Temperature	Gat			0.01		dB

ELECTRICAL CHARACTERISTICS

Phase Response

(VDD=+3.6V, VDDI=+1.8V, VSS=0V, F_{XCS}=62.5kHz, F_{MCLK}=1000kHz, F_{CCLK}=1000 kHz, Ta=+25 °C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Absolute Group Delay	Gda	f=1.0 kHz, from rising edge of XCS or 8th CCLK		2		µs
Group Delay Distortion	Gdr	f=0…20kHz, relative to Gda		0		ms

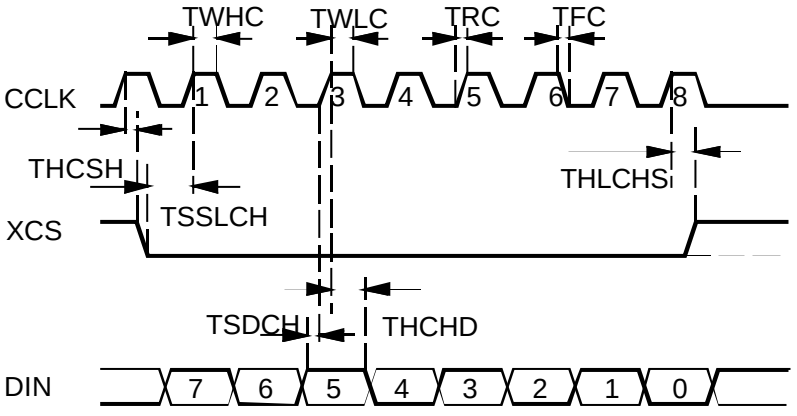
Noise and Distortion

(VDD=+3.6V, VDDI=+1.8V, VSS=0V, F_{XCS}=62.5kHz, F_{MCLK}=1000kHz, F_{CCLK}=1000 kHz, Ta=+25 °C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal to Noise and Distortion Ratio	SNR	f=1kHz, A-weight				
		100 kOhm load:				
		DIN=-1dB		45		dB
		DIN=-3dB		46		dB
		DIN=-6dB		47		dB
		8 Ohm load:				
		DIN=-1dB		42		dB
		DIN=-3dB		43		dB
		DIN=-6dB		44		dB

Serial Interface Timing Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Frequency of CCLK	FCCLK				13	MHz
Period of CCLK high	TWHC	Measured from VIH to VIH	35			ns
Period of CCLK low	TWLC	Measured from VIL to VIL	35			ns
Rise time of CCLK	TRC	Measured from VIL to VIH			10	ns
Fall time of CCLK	TFC	Measured from VIH to VIL			10	ns
Hold time, CCLK high to XCS low	THCSH		10			ns
Setup time, XCS low to CCLK high	TSSLCH		20			ns
Setup time, valid DIN to CCLK high	TSDCH		5			ns
Hold time, CCLK high to invalid CI	THCHD		10			ns
Hold time, 8th CCLK high to XCS high	THLCHS		15			ns



ELECTRICAL CHARACTERISTICS

◆ **Digital Characteristics**

DC Characteristics

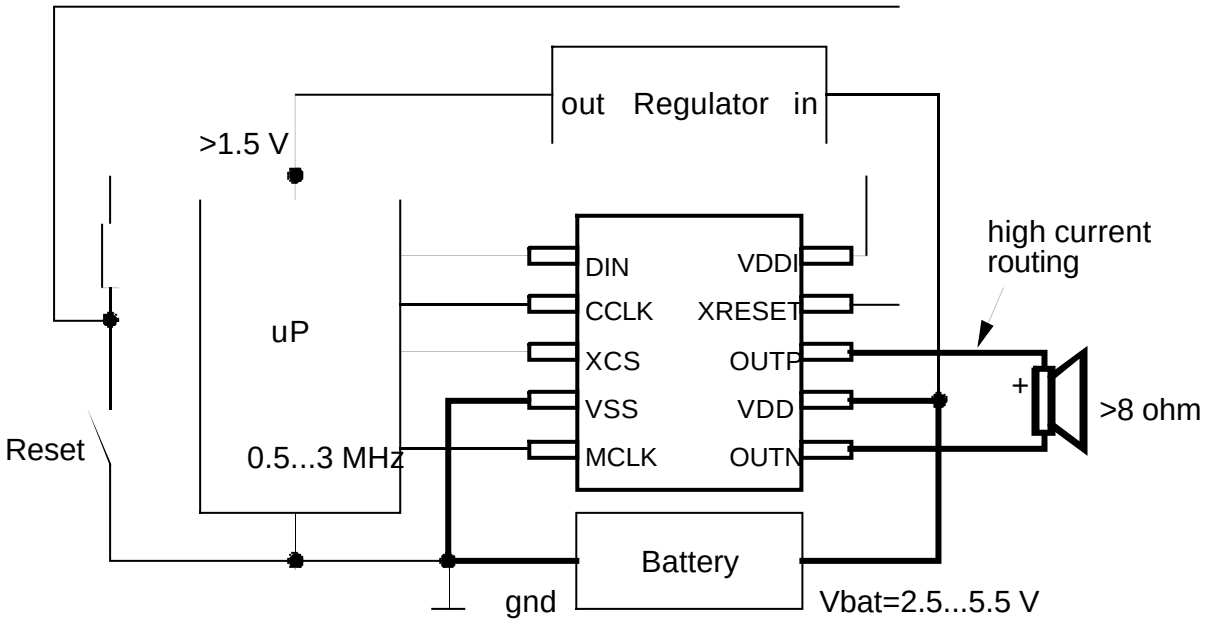
(VDD=+3.6V, VDDI=+1.8V, VSS=0V, F_{XCS}=62.5kHz, F_{MCLK}=1000kHz, F_{CCLK}=1000 kHz, Ta=+25 °C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Low Voltage	VIL	All Digital Inputs, DC	-0.3		0.3* VDDI	V
Input High Voltage	VIH	All Digital Inputs, DC	0.7* VDDI			V
Input Low Current	IL	Any Digital Input, GND<Vin<VIL	-10		10	µA

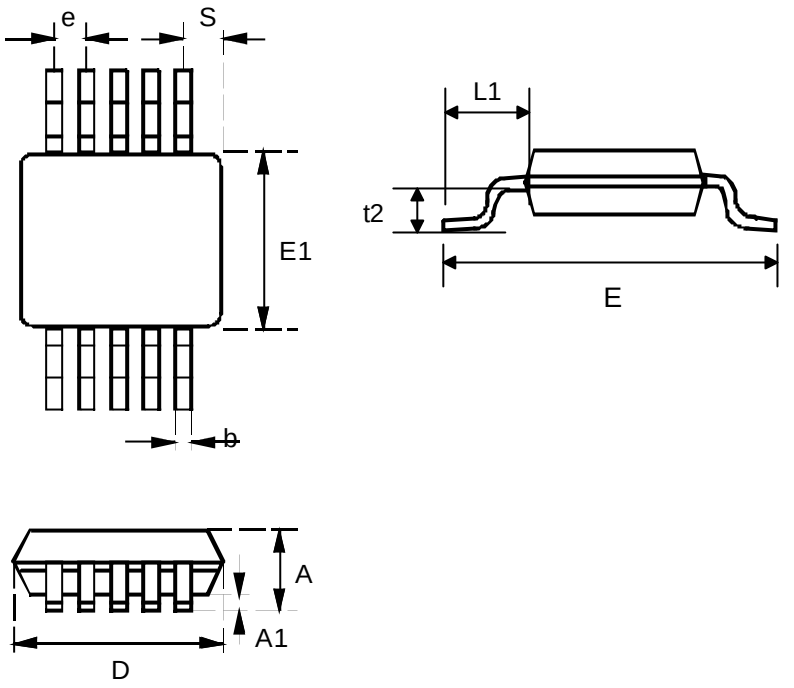
APPLICATION INFORMATION

Typical application setup is shown below. Microcontroller is controlling MAS9118 using DIN, CCLK and XCS. The microcontroller power supply is regulated voltage, which is lower than the battery voltage.

MAS9118 output drivers are directly connected to the battery voltage.The buzzer or loudspeaker can be directly connected between MAS9118 positive (OUTP) and negative (OUTN) outputs. The MAS9118 chip will automatically connect these outputs to VSS when chip is at power-down mode.



PACKAGE (MSOP10) OUTLINES



Dimension	Min	Typical	Max	Unit
A	0.95	1.00	1.10	mm
A1	0.05	0.10	0.15	mm
D	2.90	3.00	3.10	mm
E	4.75	4.90	5.05	mm
E1	2.90	3.00	3.10	mm
t2	0.33	0.41	0.49	mm
b	0.15	0.23	0.30	mm
L1		0.95		BSC
e		0.50		BSC
S		0.50		BSC

Dimensions are in accordance with Jedec standard MO-187 (excluding pitch).

ORDERING INFORMATION

Product Code	Product	Package	Comments
MAS9118ASMB-T	Buzzer DAC Interface	MSOP10	Tape and Reel

LOCAL DISTRIBUTOR

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