

MAS9275

IC FOR 10.00 - 36.00 MHz VCXO

- Low Power
- Wide Supply Voltage Range
- Square Wave Output
- Very High Level of Integration
- Very Low Phase Noise

VCXO for set-top boxes VCXO for MPEG2

Low Cost

APPLICATIONS

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DESCRIPTION

MAS9275 is an integrated circuit well suited to build VCXO for telecommunication and other

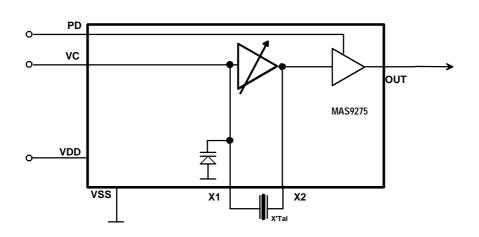
applications. To build a VCXO only one additional component a crystal is needed.

VCXO for telecommunications systems

FEATURES

- Very small size
- Minor current draw
- Wide operating temperature range
- Phase noise <-130 dBc/Hz at 1 kHz offset
- Square wave output

BLOCK DIAGRAM





PIN DESCRIPTION

Pin Description	Symbol	x-coordinate	y-coordinate	Note
Crystal/Varactor Oscillator Input	X1	209	161	
Voltage Control Input	VC	425	165	
Power Supply Ground	VSS	600	175	
Buffer Output	OUT	1029	1030	
Power Supply Voltage	VDD	841	1016	
Tri State	PD	379	1028	
Crystal Oscillator Output	X2	197	1030	

Note: Because the substrate of the die is internally connected to GND, the die has to be connected to GND or left floating. Please make sure that GND is the first pad to be bonded. Pick-and-place and all component assembly are recommended to be performed in ESD protected area.

Note: Pad coordinates are measured from the left bottom corner of the chip to the center of the pads. The coordinates may vary depending on sawing width and location, however, distances between pads are accurate.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit	Note
Supply Voltage	V_{DD} - V_{SS}	-0.3	6.0	V	
Input Pin Voltage		V _{SS} -0.3	V _{DD} + 0.3	V	
Power Dissipation	P _{MAX}		100	mW	
Storage Temperature	T _{ST}	-40	120	°C	

RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Conditions	Min	Тур	Max	Unit	Note
Supply Voltage	V _{DD}		2.5	2.8	5.5	V	1)
Supply Current	I _{DD}	VDD = 2.8 V		2.3		mA	
Operating Temperature	T _{OP}		-30		+85	°C	
Storage Temperature	Ts	Relative humidity = 15%…70%	-5		+40	°C	
Crystal Pulling Sensitivity	S			30		ppm/pF	
Crystal Load Capacitance	CL	V _C = 1.65 V		10		pF	2)

Note 1: When using the device at $VDD \ge 5$ V, we recommend connecting a 1 nF capacitor to the VDD pin.

Note 2: MAS9275A1 has a typical crystal load capacitance of 8.0 pF. MAS9275B2 has a typical crystal load capacitance of 10 pF. MAS9275B3 has a typical crystal load capacitance of 12 pF.



ELECTRICAL CHARACTERISTICS

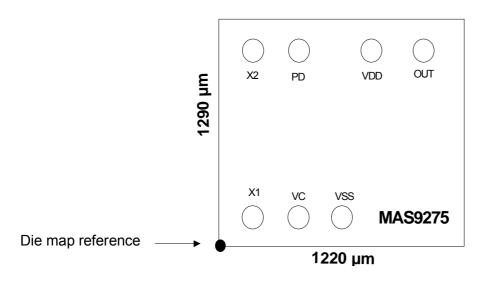
(recommended operation conditions)

Parameter	Symbol	Min	Тур	Max	Unit	Note
Frequency Range	f _o	10.00		36	MHz	1)
Voltage Control Range	V _c	0		VDD	V	
Voltage Control Sensitivity	V _{CSENS}		100		ppm/V	2)
Output Voltage (10 pF, VDD 2.7 V)	V _{out}		2.3		Vpp	
Output Voltage (10 pF, VDD 5.0 V)	V _{out}		4.5		Vpp	
Rise and Fall Time (10 - 50 pF)				10	ns	
Output Symmetry			40-60		%	
Startup Time	T _{START}		2		ms	
Tri State Output Buffer	PD				V	
ON State OFF State		0 1.6		0.55 VDD		

Note 1: An $R_s < 20 \Omega$ crystal provides 36 MHz maximum frequency. With an $R_s = 70 \Omega$ crystal the maximum frequency is typically 20 MHz.

Note 2: VC sensitivity value depends on the crystal used. With a 30 ppm/pF crystal typical values are: A1 > 100 ppm/V, B2 > 75 ppm/V, B3 > 60 ppm/V.

IC OUTLINES



Note 1: MAS9275 pads are round with 80 μm diameter at opening. **Note 2**: Die map reference is the actual left bottom corner of the sawn chip.



EXTERNAL COMPONENT SELECTION

MAS9275 requires a minimum number of external components for proper operation.

Quartz Crystal

The MAS9275 VCXO function consists of the external crystal and the integrated VCXO oscillator circuit. To assure the best system performance (frequency pull range) and reliability, a crystal device with the recommended parameters (shown below) must be used, and the layout guidelines in the following section must be followed. The frequency of oscillation of a quartz crystal is determined by its "cut" and by the load capacitors

connected to it. MAS9275 incorporates on-chip variable load capacitors that "pull" (change) the frequency of the crystal. The crystal specified for use with the MAS9275B2 is designed to have zero frequency error when the total of on-chip + stray capacitance is 10 pF (See Note 1 on page 2 for other capacitance options).

Recommended Crystal Parameters:

Initial Accuracy at 25°C ±20 ppm Temperature Stability ±30 ppm Crystal Load Capacitance 10 pf (See Note1 below) Crystal Shunt Capacitance, C0 2 pF Typical C0/C1 Ratio 300 Typical Equivalent Series Resistance 20 Ω max. Crystals with higher ESR can be used if frequency is < 36 MHz. See Note 2 under Electrical Characteristics on Page 3.

The external crystal must be connected as close to the chip as possible and should be on the same side of the PCB as the MAS9275. There should be no vias between the crystal pins and the X1 and X2 device pins. There should be no signal traces underneath or close to the crystal.

Note 1. If the crystal with a load other than 10 pF is used with MAS9275, the crystal has to have frequency offset in order to have the nominal frequency at VC = 1.65 V. Please see table below for offset frequencies vs. crystal load. (Values are for a typical crystal with S = 30 ppm/pF.)

Crystal f/MHz	19.68	19.68	27.00	40.00
Crystal Load /pF	8	10	12.5	16
Offset /ppm	+60	+5	-90	-180

Note: 19.68 MHz crystal with 10 pF load capacitance may not require frequency offset because of small deviation

For example:

For application with nominal frequency of 27.00 MHz a crystal with 12.5 pF load has to have a frequency of 27.00 MHz + $((27.00 \text{ MHz}/10^6) \times (-90)) = 26.99757 \text{ MHz}$



MODULATION RESPONSE

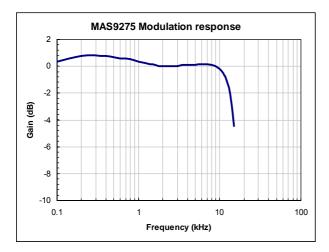


Figure 2. Modulation response (gain).

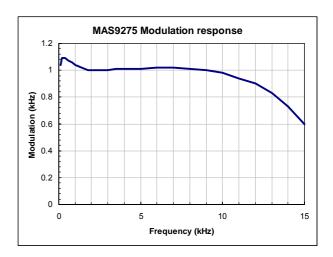
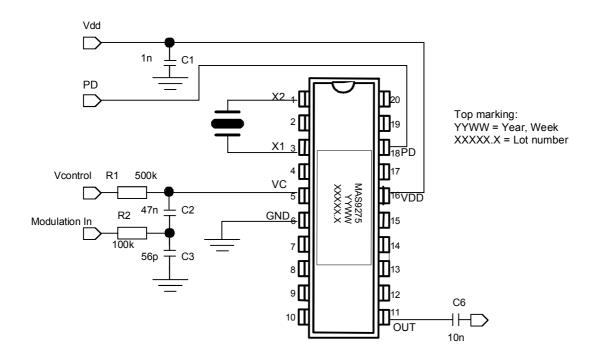


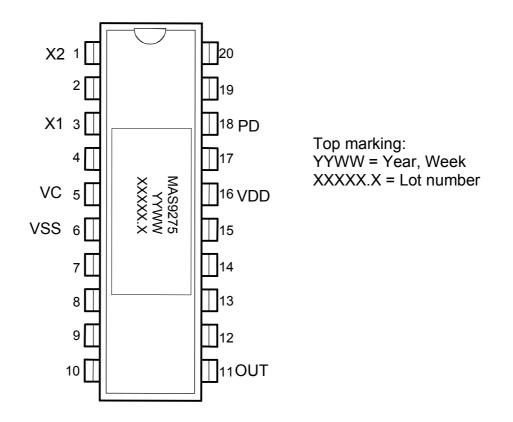
Figure 3. Modulation response (modulation).

TYPICAL APPLICATION

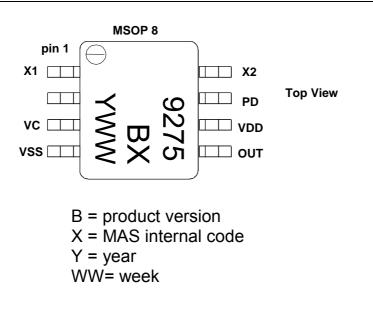




SAMPLES IN SB20 DIL PACKAGE

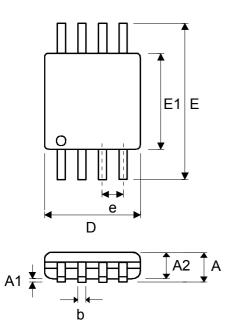


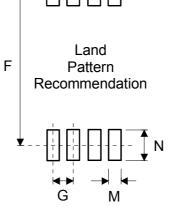
DEVICE OUTLINE CONFIGURATION

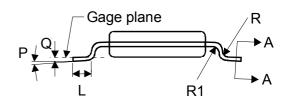


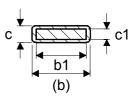


PACKAGE (MSOP-8) OUTLINE









Section A - A

Symbol	Min	Nom	Мах	Unit	
A			1.10	mm	
A1	0		0.15	mm	
A2	0.75	0.85	0.95	mm	
b	0.22		0.38	mm	
b1	0.22	0.30	0.33	mm	
С	0.08		0.23	mm	
c1	0.08		0.18	mm	
D		3.00 BSC		mm	
E			mm		
E1		3.00 BSC			
е		0.65 BSC			
F		4.8		mm	
G		0.65		mm	
L	0.40	0.60	0.80	mm	
(Terminal length for					
soldering)					
M		0.41		mm	
N		1.02		mm	
Р	0°		8°		
Q		0.25 BSC		mm	
R	0.07			mm	
R1	0.07			mm	

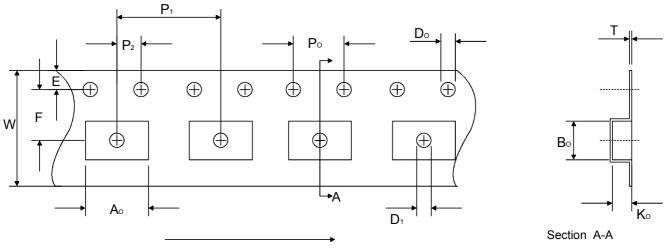
Dimensions do not include mold or interlead flash, protrusions or gate burrs. All measurement according to JEDEC standard MO-187.



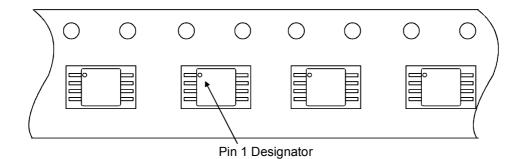
SOLDERING INFORMATION

Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20 2*220°C
Maximum Reflow Temperature	235°C
Maximum Number of Reflow Cycles	2
Seating Plane Co-planarity	max 0.08 mm
Lead Finish	Solder plate 7.62 - 25.4 μm, material Sn 85% Pb 15%

EMBOSSED TAPE SPECIFICATIONS

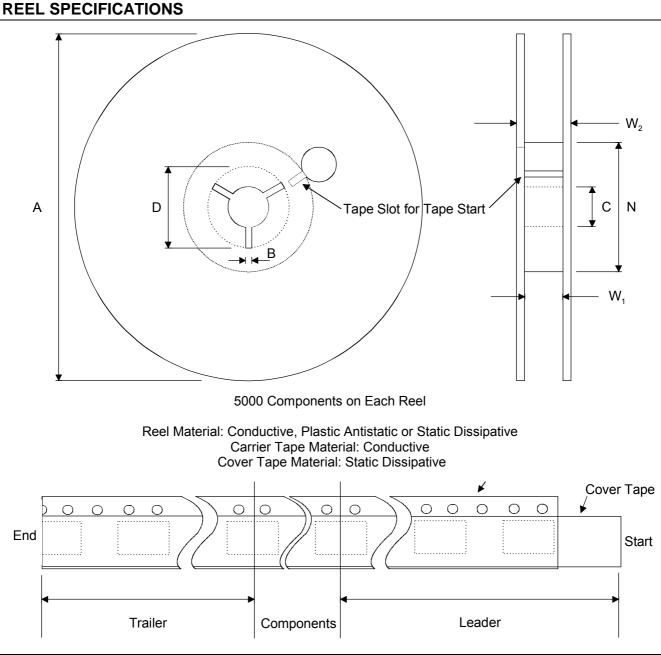


User Direction of Feed



Dimension	Min/Max	Unit
Ao	5.00 ±0.10	mm
Во	3.20 ±0.10	mm
Do	1.50 +0.1/-0.0	mm
D1	1.50 min	mm
E	1.75	mm
F	5.50 ±0.05	mm
Ко	1.45 ±0.10	mm
Po	4.0	mm
P1	8.0 ±0.10	mm
P2	2.0 ±0.05	mm
Т	0.3 ±0.05	mm
W	12.00 +0.30/-0.10	mm





Dimension	Min	Max	Unit
А		330	mm
В	1.5		mm
С	12.80	13.50	mm
D	20.2		mm
Ν	50		mm
W ₁ (measured at hub)	12.4	14.4	mm
W ₂ (measured at hub)		18.4	mm
Trailer	160		mm
Leader	390, of which minimum 160 mm of empty carrier tape sealed with cover tape		mm
Weight		1500	g



ORDERING INFORMATION

Product Code	Product	Package	Comments
MAS9275ATC1	IC FOR 2.8 V VCXO	EWS tested wafers 400 µm	Die Size 1.220 x 1.290 mm
MAS9275ATG1	IC FOR 2.8 V VCXO	EWS tested wafers 215 µm	Die Size 1.220 x 1.290 mm
MAS9275ASM1-T	IC FOR 2.8 V VCXO	MSOP-8	Tape & Reel/5000 pcs/reel
MAS9275BTC2	IC FOR 3.3 V VCXO	EWS tested wafers 400 µm	Die Size 1.220 x 1.290 mm
MAS9275BTG2	IC FOR 3.3 V VCXO	EWS tested wafers 215 µm	Die Size 1.220 x 1.290 mm
MAS9275BSM2-T	IC FOR 3.3 V VCXO	MSOP-8	Tape & Reel/5000 pcs/reel
MAS9275BTC3	IC FOR 5.0 V VCXO	EWS tested wafers 400 µm	Die Size 1.220 x 1.290 mm
MAS9275BTG3	IC FOR 5.0 V VCXO	EWS tested wafers 215 µm	Die Size 1.220 x 1.290 mm
MAS9275BSM3-T	IC FOR 5.0 V VCXO	MSOP-8	Tape & Reel/5000 pcs/reel

Please contact Micro Analog Systems Oy for other wafer thickness options.

LOCAL DISTRIBUTOR

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