v00.1204

HMC517LC4

SMT PHEMT LOW NOISE AMPLIFIER, 17 - 26 GHz

Typical Applications

The HMC517LC4 is ideal for use as a LNA or driver amplifier for:

- Point-to-Point Radios
- Point-to-Multi-Point Radios & VSAT
- Test Equipment and Sensors
- Military

Features

Noise Figure: 2.5 dB

Gain: 19 dB

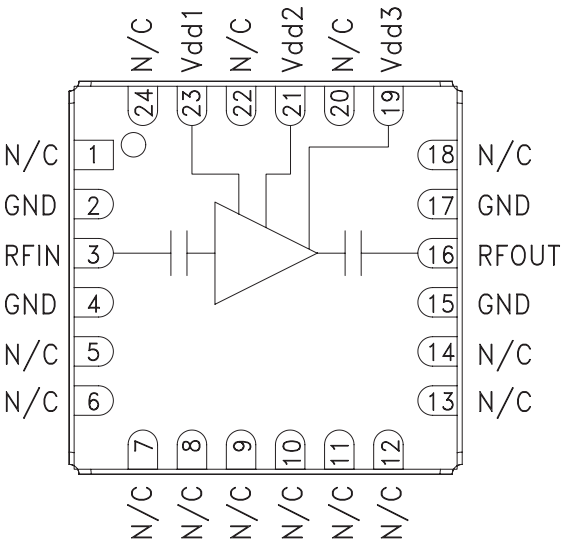
OIP3: +23 dBm

Single Supply: +3V @ 67 mA

50 Ohm Matched Input/Output

RoHS Compliant 4 x 4 mm Package

Functional Diagram



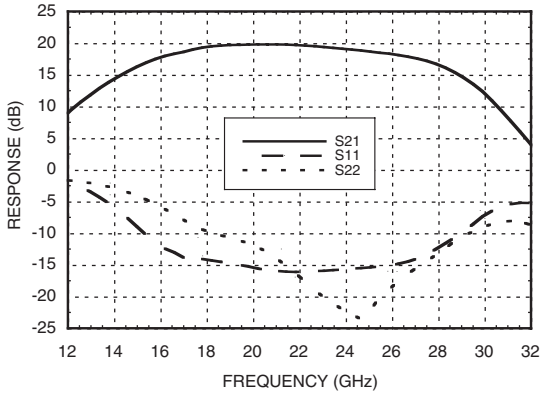
General Description

The HMC517LC4 chip is a high dynamic range GaAs PHEMT MMIC Low Noise Amplifier (LNA) housed in a leadless “Pb free” RoHS compliant SMT package. The HMC517LC4 provides 19 dB of small signal gain, 2.5 dB of noise figure and has an output IP3 of +23 dBm. The P1dB output power of +13 dBm enables the LNA to also function as a LO driver for balanced, I/Q or image reject mixers. The HMC517LC4 allows the use of surface mount manufacturing techniques.

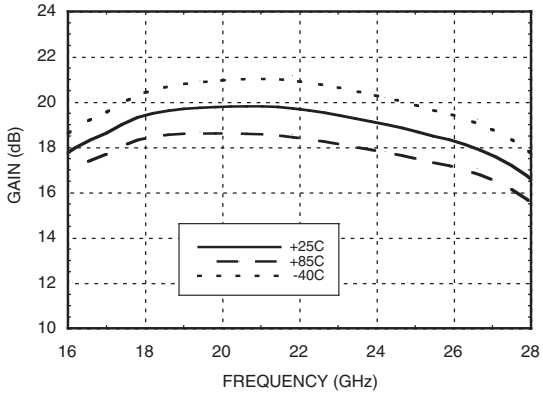
Electrical Specifications, T_A = +25° C, Vdd 1, 2, 3 = +3V

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		17 - 22			22 - 26		GHz
Gain	16	19		15	18		dB
Gain Variation Over Temperature		0.02	0.03		0.02	0.03	dB/ °C
Noise Figure		2.5	3.1		2.6	3.3	dB
Input Return Loss		15			15		dB
Output Return Loss		11			17		dB
Output Power for 1 dB Compression (P1dB)		12			13		dBm
Saturated Output Power (Psat)		15			16		dBm
Output Third Order Intercept (IP3)		23			24		dBm
Supply Current (Idd)(Vdd = +3V)		67			67		mA

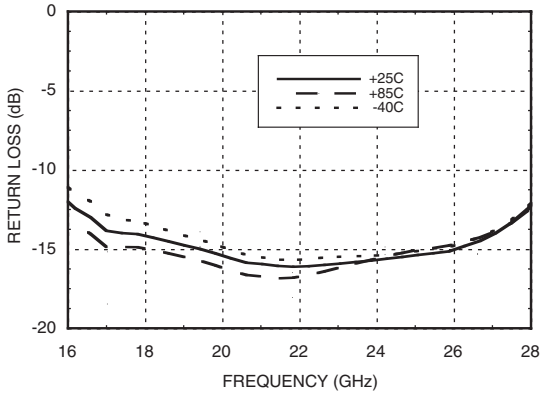
Broadband Gain & Return Loss



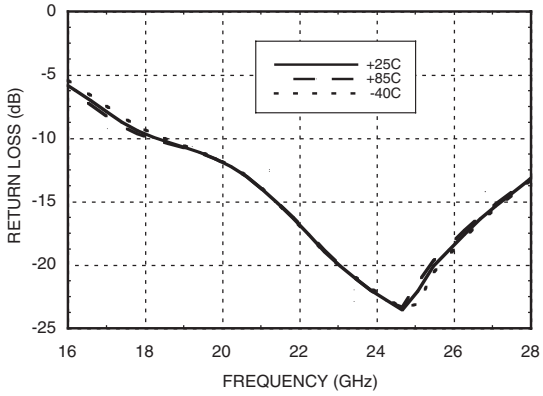
Gain vs. Temperature



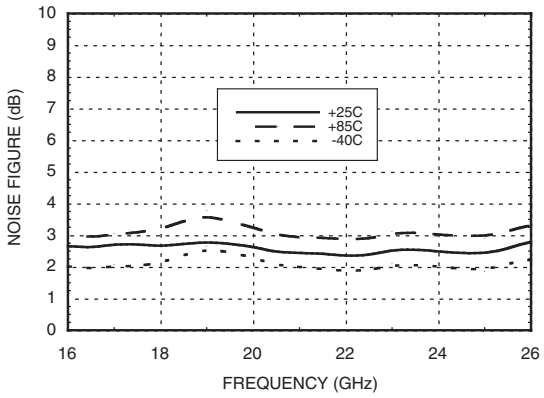
Input Return Loss vs. Temperature



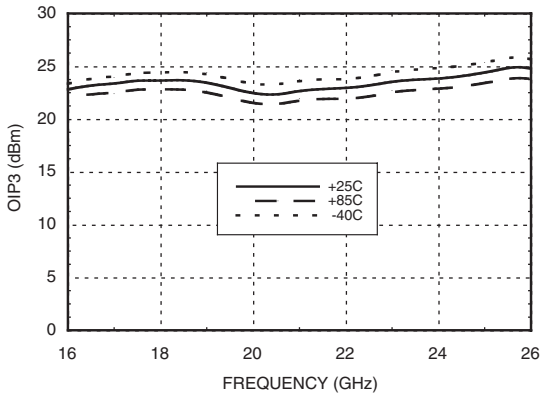
Output Return Loss vs. Temperature



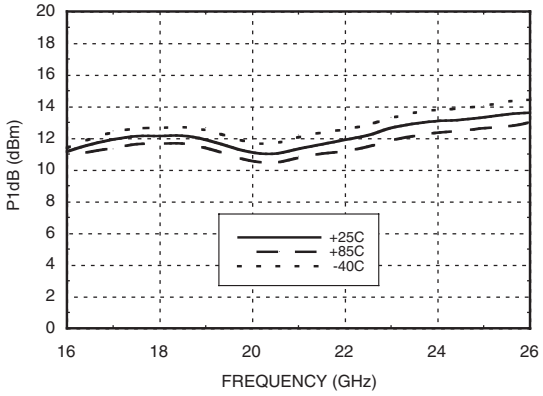
Noise Figure vs. Temperature



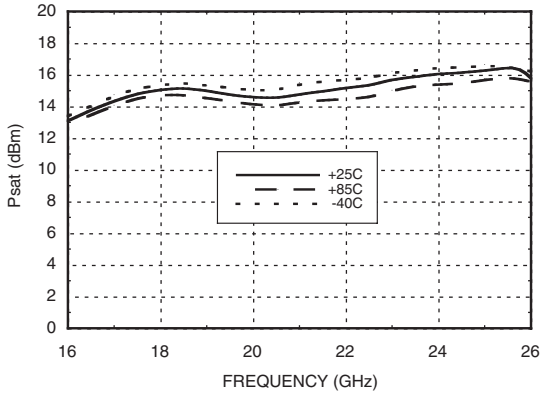
Output IP3 vs. Temperature



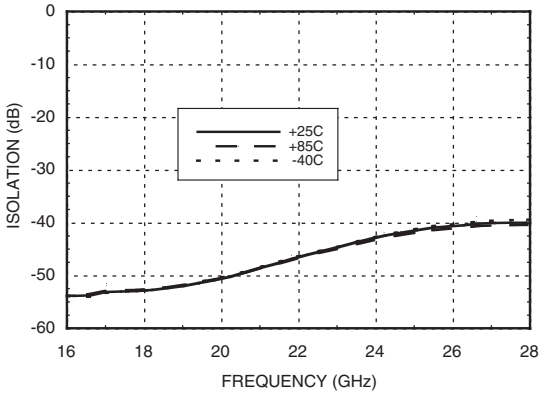
P1dB vs. Temperature



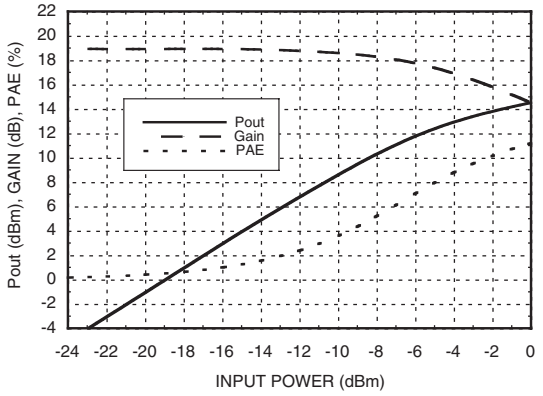
Psat vs. Temperature



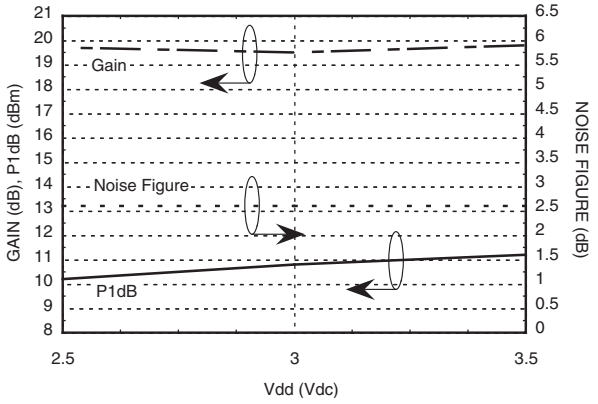
Reverse Isolation vs. Temperature



Power Compression @ 21 GHz



Gain, Noise Figure & Power vs. Supply Voltage @ 21 GHz



Absolute Maximum Ratings

Drain Bias Voltage (Vdd1, Vdd2, Vdd3)	+5.5 Vdc
RF Input Power (RFin)(Vdd = +3.0 Vdc)	+2 dBm
Channel Temperature	175 °C
Continuous Pdiss (T= 85 °C) (derate 29 mW/°C above 85 °C)	2.65 W
Thermal Resistance (channel to die bottom)	34 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

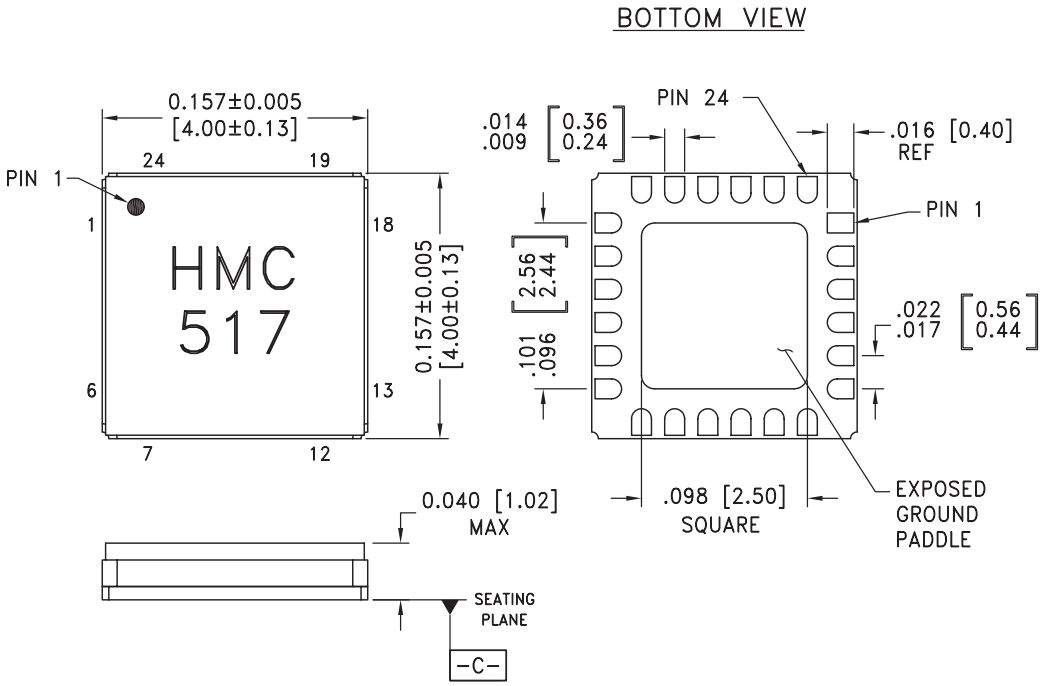
Typical Supply Current vs. Vdd

Vdd (Vdc)	Idd (mA)
+2.5	66
+3.0	68
+3.5	71

Note: Amplifier will operate over full voltage range shown above.

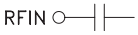
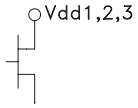
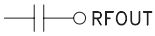
ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



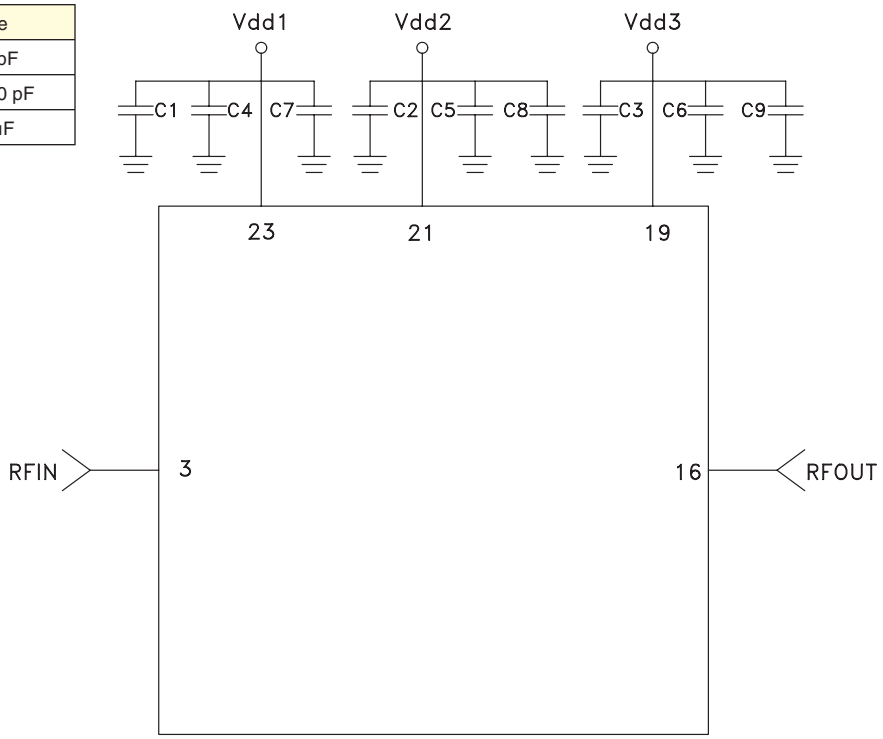
NOTES:
1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING: 30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL
3. DIMENSIONS ARE IN INCHES [MILLIMETERS]
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND

Pin Descriptions

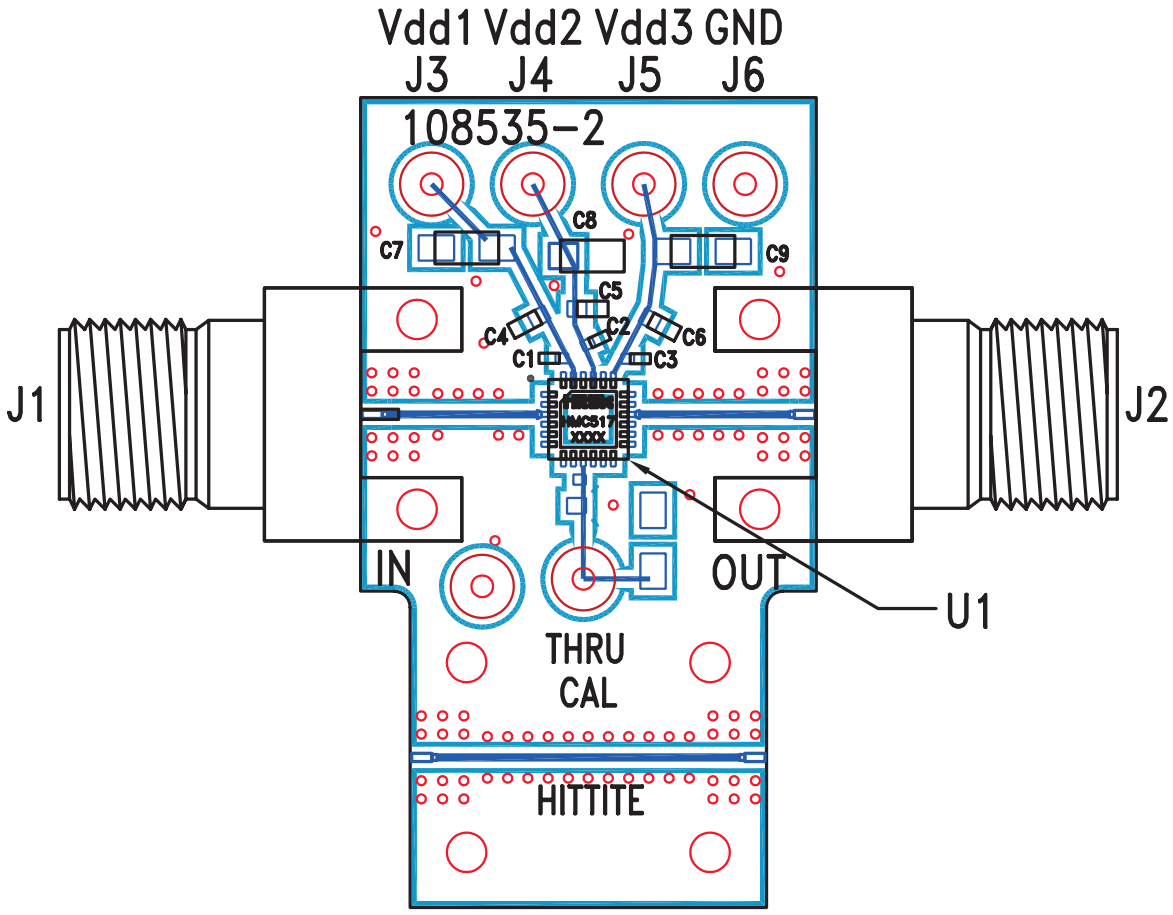
Pin Number	Function	Description	Interface Schematic
1, 5-14, 18, 20, 22, 24	N/C	This pin may be connected to RF/DC ground. Performance will not be affected.	
3	RFIN	This pin is AC coupled and matched to 50 Ohms from 17 - 26 GHz.	
23, 21, 19	Vdd1, 2, 3	Power Supply Voltage for the amplifier. External bypass capacitors of 100 pF, 1,000 pF and 2.2 µF are required.	
16	RFOUT	This pin is AC coupled and matched to 50 Ohms from 17 - 26 GHz.	
2, 4, 15, 17	GND	These pins and package bottom must be connected to RF/DC ground.	

Application Circuit

Component	Value
C1, C2, C3	100 pF
C4, C5, C6	1,000 pF
C7, C8, C9	2.2 µF



Evaluation PCB



List of Materials for Evaluation PCB 108537 [1]

Item	Description
J1 - J2	PCB Mount K Connector
J3 - J6	DC Pin
C1 - C3	100 pF Capacitor, 0402 Pkg.
C4 - C6	1,000 pF Capacitor, 0603 Pkg.
C7 - C9	2.2 µF Capacitor, Tantalum
U1	HMC517LC4 Amplifier
PCB [2]	108535 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of VIA holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.